# Bandwidth Engine® 2 Board Schematic Guidelines

Application Note AN-608

Version 0.1, July 2014
MoSys, Inc.

# Introduction

This application note describes schematic design guidelines for use with MoSys® Bandwidth Engine 2 (BE-2) devices listed in Table 1.

**Table 1 Bandwidth Engine 2 Family Devices**

| BE-2 Variant | Description |
|---|---|
| MSR620 | Burst |
| MSR720 | Access |
| MSR820 | Macro |

Schematic guidelines provided for using the Bandwidth Engine 2 devices assume a generic FPGA host as shown in Figure 1. Bandwidth Engine 2 device usage in ASIC/NPU environments is similar and can be easily derived from this document. For the purpose of this document, the FPGA is also known as host.

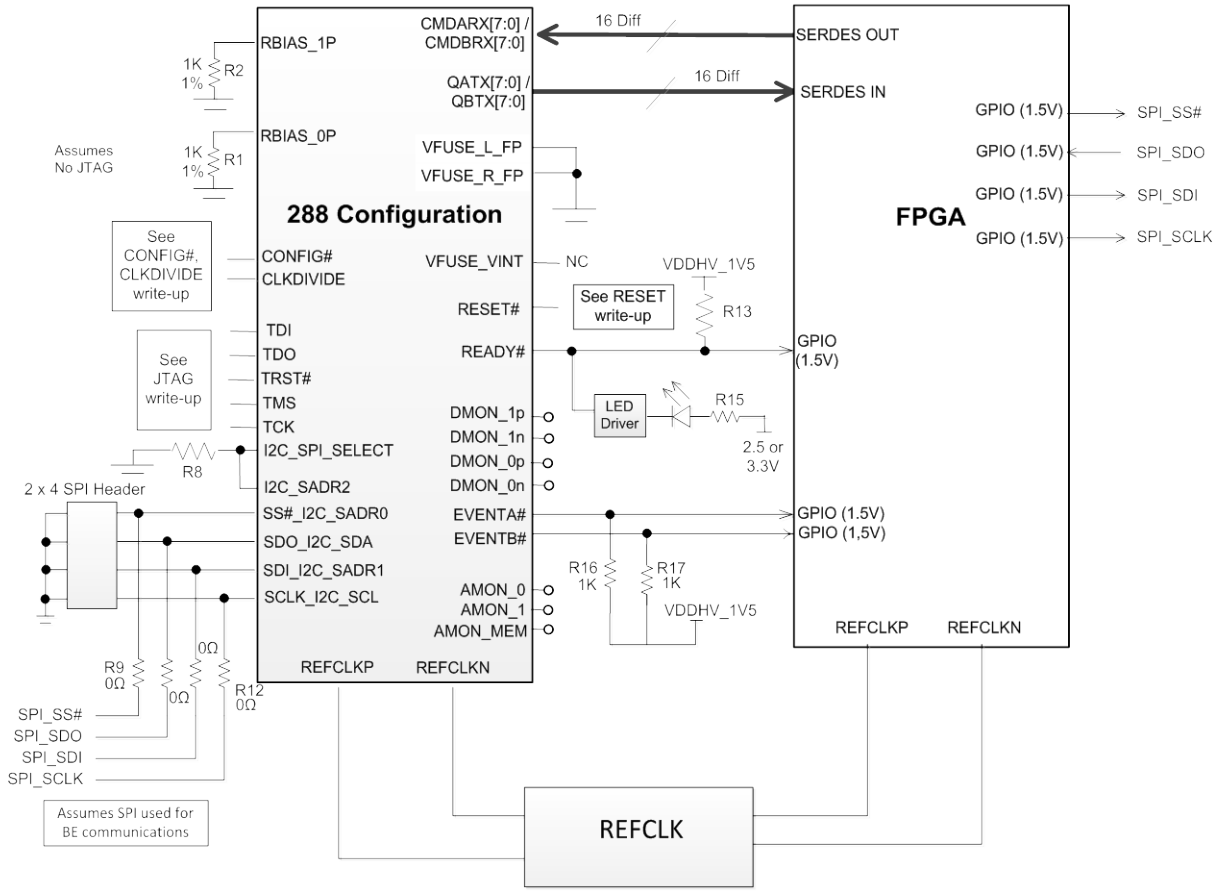
This document contains the following sections:

This document should be used in conjunction with AN-607 Bandwidth Engine 2 Board Layout Guidelines [2] which addresses signal integrity and power integrity issues.

# Suggested Interfaces Between BE-2 and Host

Figure 1 shows the connection scheme for a BE-2 device with 288 configuration. See the device datasheet for the list of pins that are not needed for the other BE-2 configurations (244, 188, and 144).

**Figure 1 Suggested interface scheme for 16 lane BE-2 device with an FPGA as SPI master**




The following sections detail the schematic design guidelines of different I/O groups on BE-2 device.

# GigaChip™ Interface (GCI) Ports

The BE-2 device supports one or two GCI ports – A and B. Each GCI port has 4 or 8 RX lanes and TX lanes. Thus there are up to 16 differential pairs connected to the

host. GCI Port A RX pairs are labeled as CMDARX while the TX differential pairs are labeled as QATX. Similarly, GCI Port B signals are labeled as CMDBRX and QBTX. The GCI port differential pairs are compatible with XFI and CEI 11G+ SR I/O standards. The I/Os support only short reach point to point connections and allows the device to be placed up to 20cm from the host.

# GCI Port Configurations

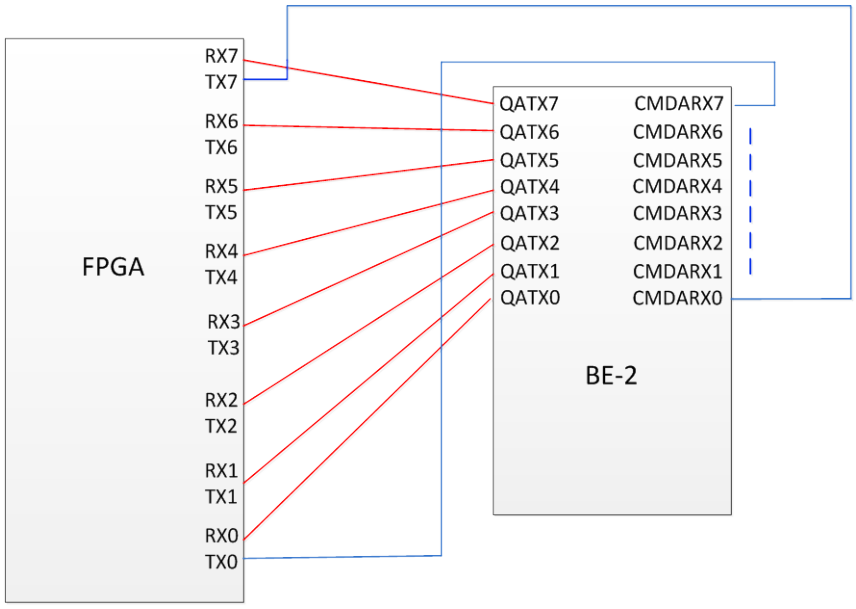
Please refer to the Selection Guide in the specific Bandwidth Engine 2 device datasheet [1] for the lane configurations that are available. Unused differential pairs in GCI port A and Port B should be left unconnected. When using both GCI ports, both ports will have the same number of RX and TX lanes.

# Lane Reordering and Polarity Inversion

To provide flexibility in routing, the BE-2 device automatically performs lane reordering and polarity inversion of the CMD*RX lanes. During training, the transmitter sends each lane's logical lane identifier on the lane. The lane identifiers control multiplexers in the receiver that steer each physical lane to the desired logical lane. The BE-2 device implements a full crossbar in each GCI port, which allows any permutation of the lanes in the host-to-BE-2 link. If the system requires reordering on the lanes from the BE-2 device to the host device, the necessary multiplexers must be designed into the host's receiver. For more information about lane reordering, see Section 3.4, "Lane Reordering," in the GigaChip Interface Specification [4].

The example in Figure 2 shows the complete reversal of the TX lanes from the FPGA to RX lanes of BE-2 device.

**Figure 2 CMDARX lanes reordering in BE-2 device**




As required by the GCI Specification, the PCS layer of both chips can detect polarity reversal for each lane and correct for the reversal.

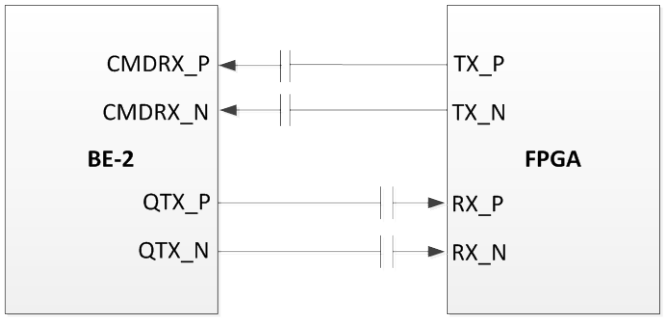
# SerDes Interface

## Choosing AC or DC Coupling

Choosing AC or DC coupling of the RX inputs is based on the signal swing and the common mode voltage. The CMDRX interface can be DC coupled if both signal swing amplitude and common mode voltage requirements are met at the RXP / RXN inputs.

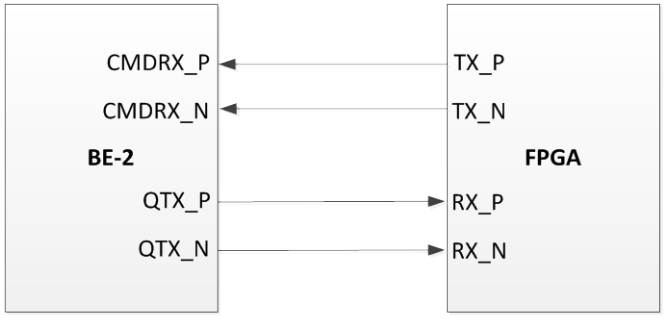
MoSys recommends connecting the SerDes interface of the BE-2 device and host in the AC coupled configuration shown in Figure 3.

**Figure 3 AC Coupling scheme for interfacing BE-2 SERDES with the FPGA**




AC coupled using 0.1uF (size 0201) capacitors

**Figure 4 DC Coupling scheme for interfacing BE-2 SERDES with the FPGA**




DC coupled without capacitors

### Signal swing of RX inputs

The conditions for AC or DC coupling of RX inputs based on signal swing are shown in Table 2.

**Table 2 Conditions for AC or DC coupling of RX inputs**

| Mode | Condition | Comments |
|---|---|---|
| AC Coupling | Any input voltage range | |
| DC Coupling | $V_{RXP}$ and $V_{RXN}$ < VDDA_SDS + 300 mV<br>and<br>$V_{RXP}$ and $V_{RXN}$ > VSS - 300 mV | AC coupling will also work for this condition |

The VDD and VDDA_SDS voltage level for each BE-2 speed grade is shown in the device datasheet [1].

Use the following equations to determine $V_{RXP}$ and $V_{RXN}$ where:

$VRX_{CM}$ is the common mode voltage at the RX inputs

Vswing_diff is the differential peak to peak voltage at the RX inputs

$V_{RXP} = VRX_{CM} + (Vswing\_diff)/4$

$V_{RXN} = VRX_{CM} + (Vswing\_diff)/4$

## Common mode voltage of RX inputs

Use Table 3 for calculating RX common mode voltage $VRX_{CM}$.

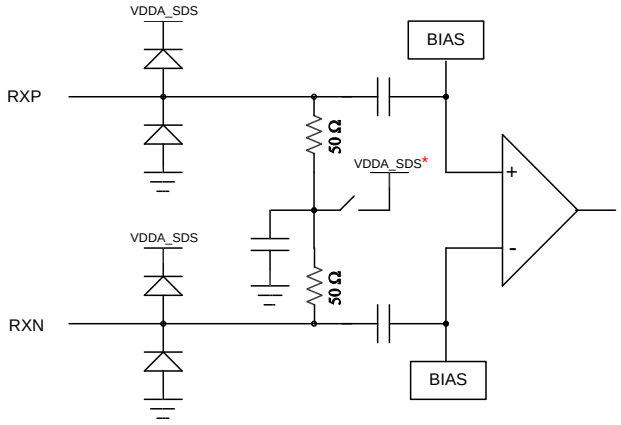
**Table 3 Calculating RX common mode voltage $VRX_{CM}$**

| Coupling Mode | Termination Common Mode | $VRX_{CM}$ | Comments |
|---|---|---|---|
| AC Coupling | VDDA_SDS | VDDA_SDS | Single-ended termination is required. |
| DC Coupling | VDDA_SDS | ($VTX_{CM}$ + VDDA_SDS)/2 | $VTX_{CM}$ is TX output common mode voltage from the host datasheet (mode = AC coupled) |
| | Float | $VTX_{CM}$ | |

## Termination common mode of RX inputs

The CMDRX input circuitry with selectable termination is shown in Figure 5.

**Figure 5 CMDRX input circuit**




*Termination common mode can be to VDDS_SDS (default) or floating.

To determine the appropriate termination common mode for the RX inputs use Table 4.

**Table 4 Determining termination common mode for RX**

| Coupling Mode | $VRX_{CM}$ | Termination Common Mode | Comments |
|---|---|---|---|
| AC Coupling | Any Common mode voltage | VDDA_SDS | Single-ended termination is required. |
| DC Coupling | VDDA_SDS>$VRX_{CM}$ > 0.65 | VDDA_SDS | Typically used for CML drivers |
| | 0.4 <= $VRX_{CM}$ <= 0.65 | Float | Reduces power, typical for voltage mode drivers |

The termination common mode is selected through a control register via SPI/I2C interface and can be changed using the poke command.

The default setting is with the termination common mode to VDDA_SDS

```
poke pma_sl_spare.pcs_sds_slice_spare 0x80000  #To terminate to VDDA_SDS
poke pma_sl_spare.pcs_sds_slice_spare 0x00000  #To terminate to floating
```

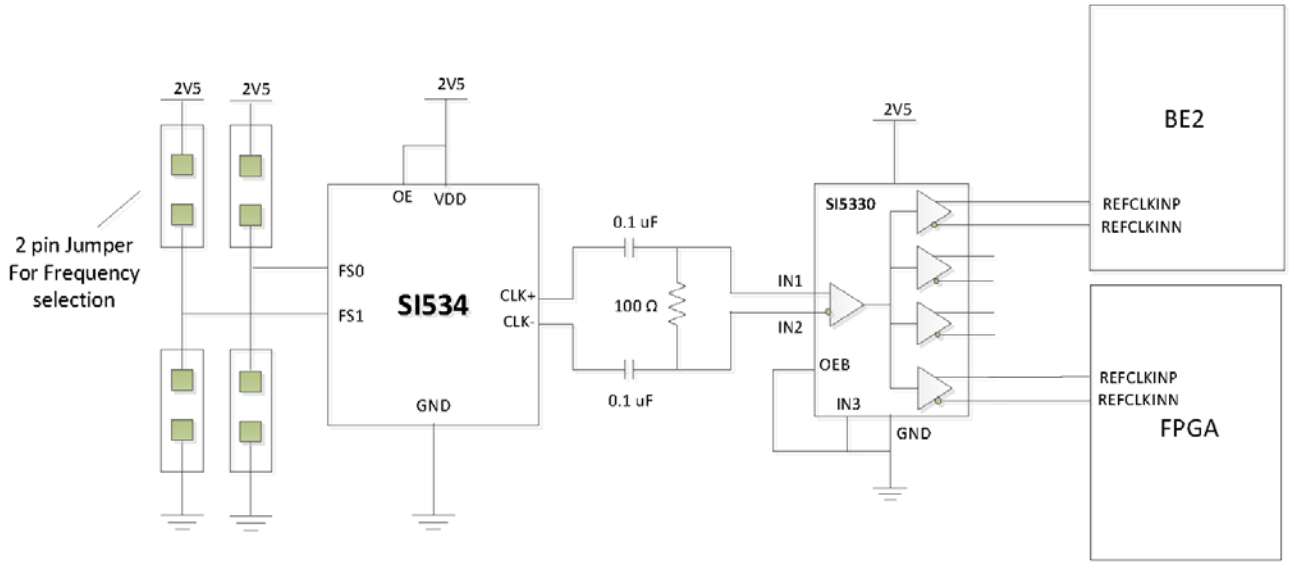
# SERDES Bias Signals

BE-2 SerDes requires separate external bias resistors for each GCI port on RBIAS_0P/1P pins as shown in Figure 1. These RBIAS resistors require a value of 1 kΩ with 1% tolerance and they should be placed directly under or adjacent to the BGA footprint. Please refer to the Bandwidth Engine 2 Board Layout Guidelines application note [2] for the RBIAS resistor layout details.

# Reference Clock

The BE-2 device uses the common reference clock scheme. The clock for BE-2 device and the host controller must be derived from the same source. Figure 6 shows a recommended reference clock circuit for the BE-2 device. The SI534 clock chip is available from Silicon Labs.

**Figure 6 Recommended Reference clock circuit for BE-2 device**




The BE-2 reference clock inputs can be directly driven by any LVDS fanout buffer as long as it meets the jitter and rise time requirements. Please refer to the device datasheet [1] for the actual jitter and rise time specifications. Further, the maximum output common mode voltage of LVDS fanout buffer must be less than 1.3V. AC coupling capacitors should be used at the BE-2 reference inputs if the output common mode voltage of the LVDS fanout buffer is higher than 1.3V.

Table 5 lists the possible BE-2 data rates with four example reference clock frequencies.

**Table 5 BE-2 REFCLK frequency and multiplier examples**

| REFCLK = 125 MHz | | REFCLK = 156.25 MHz | | REFCLK = 175.625 MHz | | REFCLK = 312.5 MHz | |
|---|---|---|---|---|---|---|---|
| CLKDIVIDE is Low | | CLKDIVIDE is Low | | CLKDIVIDE is Low | | CLKDIVIDE is High | |
| Multiplier | Data Rate (Gbps) | Multiplier | Data Rate (Gbps) | Multiplier | Data Rate (Gbps) | Multiplier | Data Rate (Gbps) |
| 33 | 8.2500 | 27 | 8.4375 | 24 | 8.4300 | 27 | 8.4375 |
| 34 | 8.5000 | 28 | 8.7500 | 25 | 8.7813 | 28 | 8.7500 |
| 35 | 8.7500 | 29 | 9.0625 | 26 | 9.1325 | 29 | 9.0625 |
| 36 | 9.0000 | 30 | 9.3750 | 27 | 9.4838 | 30 | 9.3750 |
| 37 | 9.2500 | 31 | 9.6875 | 28 | 9.8350 | 31 | 9.6875 |
| 38 | 9.5000 | 32 | 10.0000 | 29 | 10.1863 | 32 | 10.0000 |
| 39 | 9.7500 | 33 | 10.3125 | 30 | 10.5375 | 33 | 10.3125 |
| 40 | 10.0000 | 34 | 10.6250 | 31 | 10.8888 | 34 | 10.6250 |
| 41 | 10.2500 | 35 | 10.9375 | 32 | 11.2400 | 35 | 10.9375 |
| 42 | 10.5000 | 36 | 11.2500 | 33 | 11.5913 | 36 | 11.2500 |
| 43 | 10.7500 | 37 | 11.5625 | 34 | 11.9425 | 37 | 11.5625 |
| 44 | 11.0000 | 38 | 11.8750 | 35 | 12.2938 | 38 | 11.8750 |
| 45 | 11.2500 | 39 | 12.1875 | 36 | 12.6450 | 39 | 12.1875 |
| 46 | 11.5000 | 40 | 12.5000 | 37 | 12.9963 | 40 | 12.5000 |
| 47 | 11.7500 | 41 | 12.8125 | 38 | 13.3475 | 41 | 12.8125 |
| 48 | 12.0000 | 42 | 13.1250 | 39 | 13.6988 | 42 | 13.1250 |
| 49 | 12.2500 | 43 | 13.4375 | 40 | 14.0500 | 43 | 13.4375 |
| 50 | 12.5000 | 44 | 13.7500 | 41 | 14.4013 | 44 | 13.7500 |
| 51 | 12.7500 | 45 | 14.0625 | 42 | 14.7525 | 45 | 14.0625 |
| 52 | 13.0000 | 46 | 14.3750 | 43 | 15.1038 | 46 | 14.3750 |
| 53 | 13.2500 | 47 | 14.6875 | 44 | 15.4550 | 47 | 14.6875 |
| 54 | 13.5000 | 48 | 15.0000 | | | 48 | 15.0000 |
| 55 | 13.7500 | 49 | 15.3125 | | | 49 | 15.3125 |
| 56 | 14.0000 | 50 | 15.6250 | | | 50 | 15.6250 |
| 57 | 14.2500 | | | | | | |
| 58 | 14.5000 | | | | | | |
| 59 | 14.7500 | | | | | | |
| 60 | 15.0000 | | | | | | |
| 61 | 15.2500 | | | | | | |
| 62 | 15.5000 | | | | | | |

# SPI/I2C and JTAG Ports

## SPI/I2C Port

The BE-2 SPI/I2C port is required for chip configuration and status monitoring. It can be directly connected to the FPGA or control/management plane processor with 1.5V LVCMOS compatible IOs.

The I2C_SPI_SELECT input pin selects between the SPI interface and the I2C interface. The signals for these ports share the same package pins. If the I2C_SPI_SELECT input is high at reset, the I2C interface is selected. If the input is low at reset, the SPI interface is selected. See the device datasheet for more details of reset requirements.

### SPI Interface

For debug purposes, we connect the SPI signals to a 2 x 4 or 1 x 6 header as shown in Figure 1. If the header cannot be accommodated then make the zero ohm resistors size 0603. For debug of boards without a header the 0603 resistors can be removed and wires soldered on the pads in order to drive the SPI signals independent of the host device. If using a header make sure that it can connect to the selected dongle. The recommended USB to SPI host adapter is the Total Phase Cheetah. The Cheetah dongle has 10 pins on its connector and is keyed. A level translator circuit (SN74AVC4T774 or equivalent) must be used if the SPI master does not provide 1.5V LVCMOS I/Os.

The link below is to the Cheetah website.
http://www.totalphase.com/products/cheetah_spi/

### I2C Interface

We recommend using SPI interface for BE-2 communication which has been verified per the device datasheet requirements. Even if I2C interface is selected for BE-2 communication the SPI interface should be correctly wired so it can be used as a backup to I2C interface.

The I2C interface has the following characteristics:

- Maximum frequency of 100 KHz
- Clock stretching option not supported
- Upper 4 bits of BE-2 I2C address are hardwired to 4'b0100, lower 3 bits are set by package pins at reset

See the device datasheet for additional information on the I2C Interface.

## JTAG Port

The JTAG port is not normally required for BE-2 device bring up or debug. Hence, the main application for the JTAG port is boundary scan. Table 6 lists the JTAG functions needed for boundary scan. If the JTAG port is not used TRST# and TCK pins must be pulled down using 1K resistors.

**Table 6 JTAG functions**

| Pin | JTAG Function | Comments |
|---|---|---|
| TCK | Clock | Must be held Low if JTAG not used. |
| TMS | Mode Select | May be left unconnected if JTAG not used |
| TRST# | Reset | Must be held Low except during JTAG operations |
| TDI | Data In | May be left unconnected if JTAG not used |
| TDO | Data Out | May be left unconnected if JTAG not used |

# Initial Board Bring-up and Debug Signals

We recommend using the following signals on the board for BE-2 device bring up and debug purposes,

## AMON

There are three AMON pins (AMON_0, AMON_1, AMON_MEM) on the BE-2 device that monitor internal analog voltages. These AMON pins can be helpful for debugging the SERDES and MoSys recommends connecting to test points on the PCB as shown in Figure 1.

## DMON

There are two DMON differential pairs (DMON_0P/N and DMON_1P/N) on the BE-2 device corresponding to the two GCI ports. They are used to monitor internal SerDes related high-speed signals and MoSys recommends connecting to SMA connectors or test points. DMON signals are shown in Figure 1 as test points.

# Miscellaneous Signals

The miscellaneous signals in BE-2 device can be classified in three groups: Initialization, VFUSE, and status monitors. The board design requirements for these three signal groups are described below.

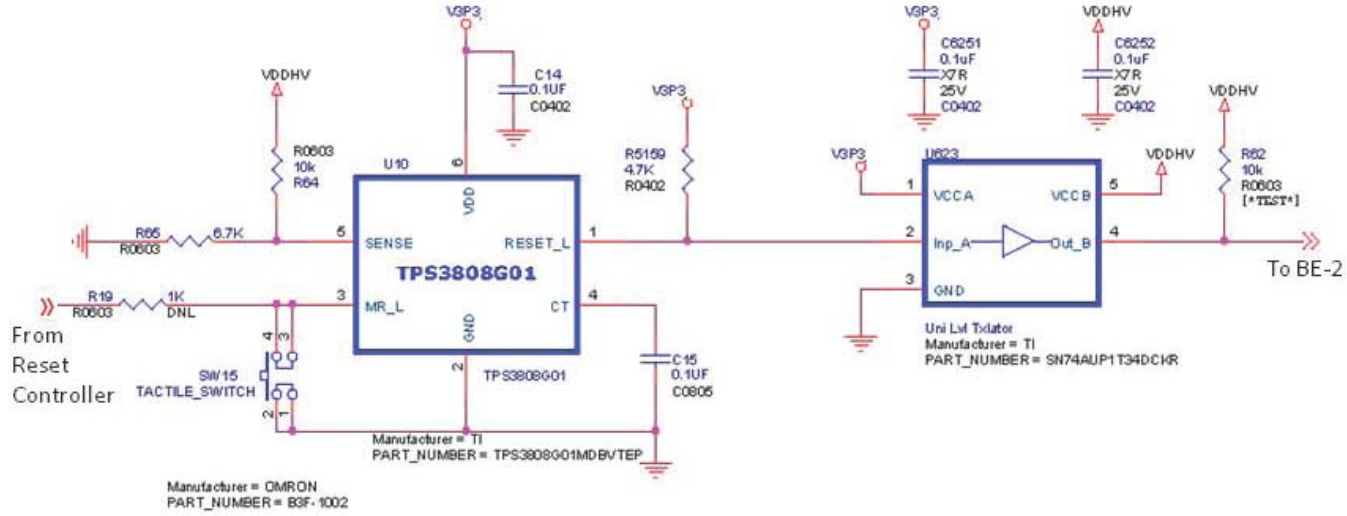
## Initialization Signals

The BE-2 initialization signals are RESET#, CONFIG#, and CLKDIVIDE.

### RESET#

For board bring-up and debug, MoSys recommends adding a Programmable Delay Supervisory circuit like the TPS3808 IC shown in Figure 7 followed by a level translator circuit (SN74AUP1T34). The level translator is needed to change the signal level to 1.5V and to meet the 20 ns Reset rise time specification in the device datasheet and AN-609. A manual push reset switch as shown in Figure 7 will also help for debug and board bring-up.

**Figure 7 Reset Circuit**




In addition to the above hardware RESET, it is also recommended to reset the BE-2 device when any of its supply voltage falls below its specified minimum voltage. Further, the BE-2 reset input should be held in the asserted state for at least 0.01 ms after the power supplies and REFCLK are in spec. A reset monitor circuit can be used for this purpose.

Please consult the device datasheet [1] and the Power-up and Reset AN-609 [3] for the requirements on reset duration, rise and fall times.

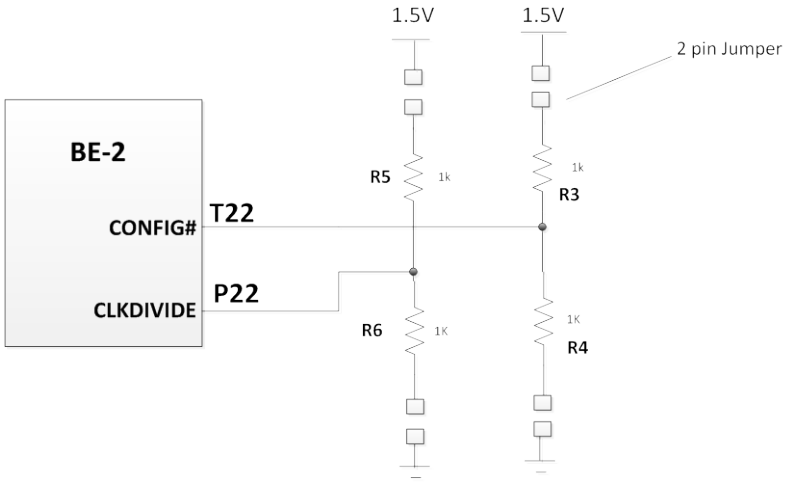
## CONFIG# and CLKDIVIDE

During reset, CONFIG# provides a method to use the SPI/I2C port to override the default configuration of the device (such as setting up the PLL clock multiplier). A Low value causes the PLL initialization to be held off until the CONFIG_DONE bit in register rstgen_rst is set via the SPI/I2C port. A High signal causes the default values for all registers to be loaded and the PLL initialization to proceed automatically upon de-assertion of RESET#.

Asserting CLKDIVIDE during reset causes the external reference clock frequency to be divided by 2 (for example, a 312.5 MHz external REFCLK becomes an internal 156.25 MHz REFCLK). A Low value causes the divide circuit to be bypassed. The CLKDIVIDE pin is held Low for reference clock frequencies lower than 200 MHz and it is held High for frequencies above 200 MHz.

It is recommended to use both pull up (R3/R5) and pull down resistors (R4/R6) for the CONFIG# and CLKDIVIDE pins on the board as shown in Figure 8. The pull up or pull down resistors can be stuffed appropriately per the desired reset configuration. Jumpers as shown in Figure 8 can add flexibility for the BE-2 reset configuration.

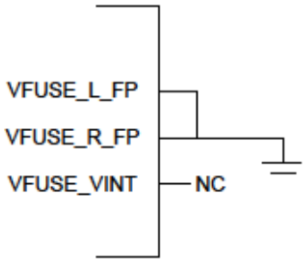
**Figure 8 BE-2 reset configuration using 2 jumpers on the board**




# VFUSE

The Bit Safe® memory repair feature has options for soft repair and hard repair of defective memory bits. BE-2 devices have three VFUSE pins to support hard repair. If the board does not need to support hard repair the VFUSE pins should be wired as shown in Figure 9. Pins VFUSE_R_FP and VFUSE_L_FP need to be connected to ground. Pin VFUSE_VINT needs to be left unconnected.

**Figure 9 VFUSE pin connections**




For more details on Bit Safe memory repair in general and the hardware configuration needed for hard repair support, see erratum #52 in the Bandwidth Engine 2 Errata list [5].

# Status Monitor Signals

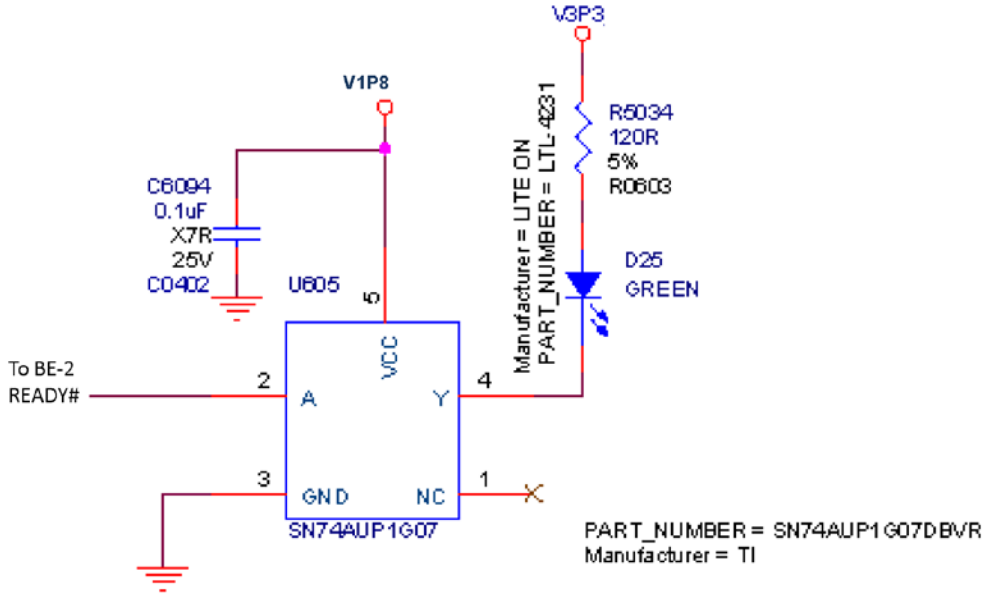
There are 3 status output pins on BE-2 device namely READY#, EVENTA# and EVENTB#.

## READY#

The READY# output is asserted Low to indicate the device has completed configuration. Lane training begins automatically. When training is complete the device is ready to receive commands over the CMDARX and CMDBRX interfaces. The READY# signal is very useful for BE-2 device bring-up and debug. It is recommended to use a LED for the READY# pin for visual status of the BE-2 device. The READY# pin requires an external LED driver as it supports only 1.5V LVCMOS

IO. A Reference LED driver circuit using a TI driver is shown in Figure 10. The READY# output of BE-2 is open-drain and needs a pull-up resistor to VDDHV.

**Figure 10 Reference LED driver circuit for monitoring READY# pin status**




## EVENTA# and EVENTB#

The EVENTA# and EVENTB# pins are used to indicate an event has been posted to a Status Register.

The EVENT# outputs are open drain and need a pull-up resistor to VDDHV. The board configuration shown in Figure 11 can be used with one or two event pins, with or without wire-ORing. Table 7 shows which resistors to populate for each configuration.

If the EVENT# pins are used for high speed signaling from BE-2 to the controller, it is recommended that the EVENT# pins be routed as short a trace as possible back to the controller. This is to minimize timing delays from EVENT# to the host controller recognizing EVENT#.
See the Bandwidth Engine 2 Board Layout Guidelines AN-607 [2] for further board routing recommendations.

**Figure 11 EVENT# pin connections**

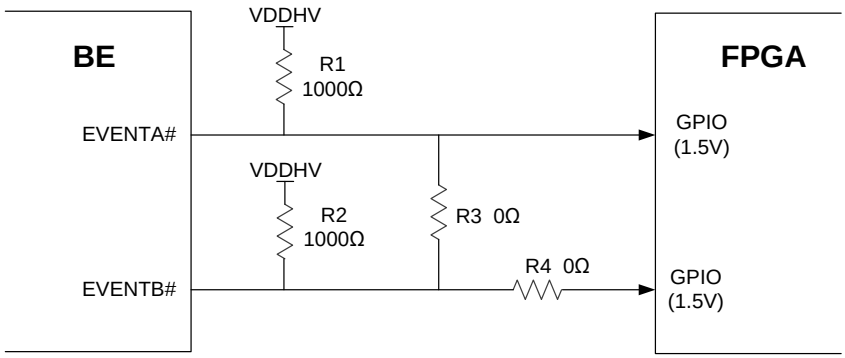


**Table 7 Event pin connection options**

| Event pins used | FPGA Connection | Populate These Resistors |
|---|---|---|
| 1 | One input pin. | R1 or R2 |
| 2 | One input pin. Wire-OR configuration | R1, R3 |
| 2 | Two input pins | R1, R2, R4 |

# Die Temperature Monitoring

It is critical to maintain the BE-2 device case temperature below the datasheet limit for proper operation. The maximum case temperatures are 85°C (Commercial) or 100°C (Extended). In order to monitor die temperature, the BE-2 device provides a thermal diode interface which can be connected to a temperature monitor circuit as shown in Figure 12. The ON Semi ADT7461 device has a built in ADC through which digital equivalent of on-die temperature can be read via the I2C interface. Note that the BE-2 thermal diode interface pins (TEMPDIODEP/N) can be left open if the temperature monitor is not used.

## Temperature diode calibration

To calibrate the ADT7461 temp diode circuit perform the following:

- First remove diode temp sensor and any other load on the BE-2 temp diode pins.
- Then source 20uA across BE-2 temp diode pins (use Keithley 6220 current source or equivalent). Measure VBE across temp diode pins and calculate BE2 die temp using below formula:

  T = (765.88-VBE)/1.753 where VBE is the voltage in mV measured across the diode at 20µA.

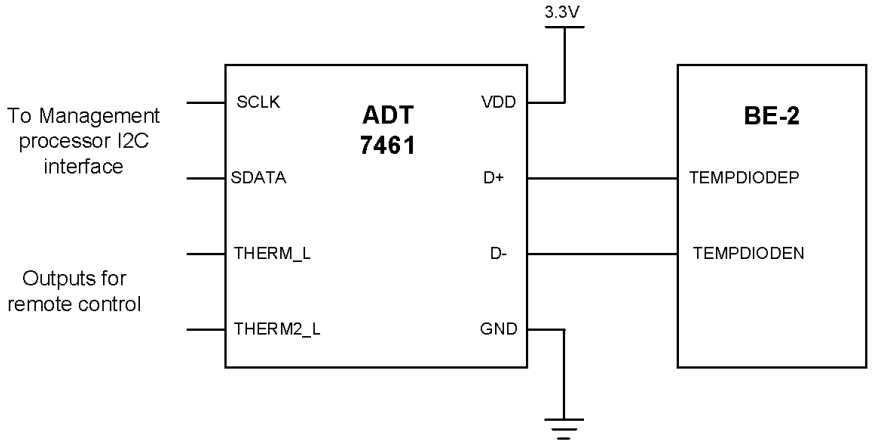
  This should agree with a thermocouple reading within a few degrees.
- Next reinstall the removed components and program the diode temp sensor device so the output reads the temperature calculated above.

If using a different temperature monitor circuit the following generalized formula (for arbitrary Id) can be used with a maximum source current of 50uA:

T = (691.99 + 24.562 * ln(Id) - VBE / (2.0058 - 0.0841 * ln(Id) ))

Using either formula, this technique should be accurate within a few % from 25°C to 125°C. It is most accurate when BE-2 is not operating. If BE-2 is actively writing/reading, the equation can be off by more than 10°C (usually higher than the actual temperature).

**Figure 12 Reference Die temperature monitor circuit for BE-2 device**



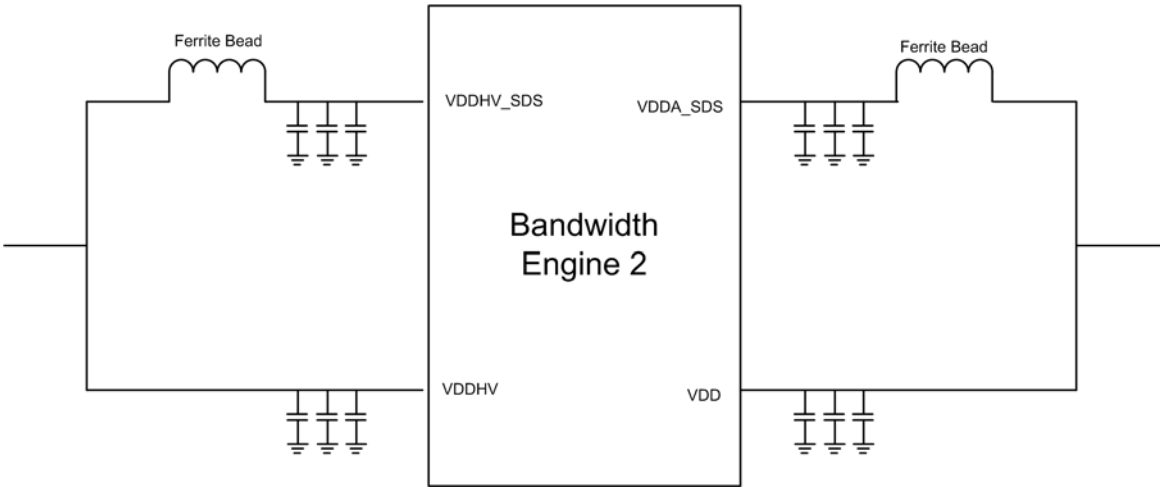

# Power Supply

The four power supplies can be generated separately or 2 board supplies can generate the needed voltage levels (as shown in Figure 13).

If the board does not need to support hard repair and the VFUSE pins are connected according to Figure 9, then there are no restrictions for the sequence that the power supplies and REFCLK come up. Figure 13 shows the recommended power supply scheme for the Bandwidth Engine 2 device.

We recommend using a linear Low Drop Out (LDO) voltage regulator for the SERDES supplies. SERDES power supply domains should be filtered using ferrite beads unless a dedicated voltage regulator is used. For information on power routing guidelines see Bandwidth Engine 2 Board Layout Guidelines AN-607 [2].

**Figure 13 Recommended Power Supply Scheme for Bandwidth Engine devices**



# Ferrite Bead Selection

If one power supply generates both VDD and VDDA_SDS or both VDDHV and VDDHV_SDS then a ferrite bead ~47nH or larger is required to isolate the _SDS power supply from the non SerDes power supply. The DC resistance will have IR drop that needs to be accounted for in the power delivery. Low DC resistance should be used. Connecting the power supply sense lines to BE-2 will compensate for the voltage drop of the ferrite bead.

An example bead, Murata BLM18S Series bead, is described below, but customer can choose the value and component based on their individual power supply budgets, and how many BE chips are being supplied.

The characteristics of the recommended ferrite bead for filtering the VDDA_SDS and VDDHV_SDS domains is shown in Table 8.

**Table 8 Recommended ferrite bead**

| Characteristic | Value |
|---|---|
| Manufacturer Part number | BLM18SG700TN1D |
| Manufacturer | Murata (www.murata.com) |
| Current rating | 4.0A |
| DC Resistance | 20 mΩ |
| AC resistance | 70 Ω @ 100 MHz |
| Body size | 0603 |

http://search.murata.co.jp/Ceramy/image/img/PDF/ENG/L0110S0100BLM18S.pdf

## Example Calculations

This example is for a MSR620ACC288-12 device and the VDDA_SDS power supply. It calculates the maximum ferrite bead resistance of the 0.95 volt VDDA_SDS supply where Rfb is the resistance of the ferrite bead. See the device datasheet for all the power supply specifications.

Rfb < (Vsupply - Vmin) / Ivdda_sds.
Where Vmin is 0.903 V and Ivdda_sds = 1.5 A for 288 configured device
Rfb< .047/1.5 = 0.031 ohms

Important factors for selecting ferrite beads are current capacity, DC resistance and AC impedance. The AC impedance is usually specified at 100 MHz. Although ferrite beads with high AC impedance may seem better for noise suppression, they may cause the power supply network to resonate. Ferrite beads that have higher AC impedance tend to have higher DC resistance as well. This DC resistance can cause excessive IR drop leading to the device failure.

# Decoupling Requirements

Decoupling capacitors are required on the board to meet the power supply noise specifications. There are two methodologies to estimate decoupling capacitor requirements on the board. The simplest approach is to add a high frequency decoupling capacitor (typically 0.1 uF) per power supply pin. Place these high frequency decoupling capacitors under the Bandwidth Engine 2 BGA footprint for

maximal effectiveness. Please refer to AN-607 for further details on the placement of high frequency decoupling capacitors.

In addition to high frequency decoupling capacitors, bulk decoupling capacitors are required for low frequency decoupling. Typically, a network of capacitors in parallel of values ranging from 1 uF to 470 uF forms an effective bulk decoupling solution.

Although the approach described above is simple to implement, it may lead to using more capacitors than required. The second method to derive the on-board decoupling requirements is to use the target impedance method which optimizes the number of capacitors required. In this method, an impedance target is defined separately for each power supply domain. The impedance target is met by adding the appropriate number of capacitors, typically using EM simulators such as Power-SI or SIWAVE. Please refer to AN-607 for the target impedance specification for Bandwidth Engine 2 device power domains.

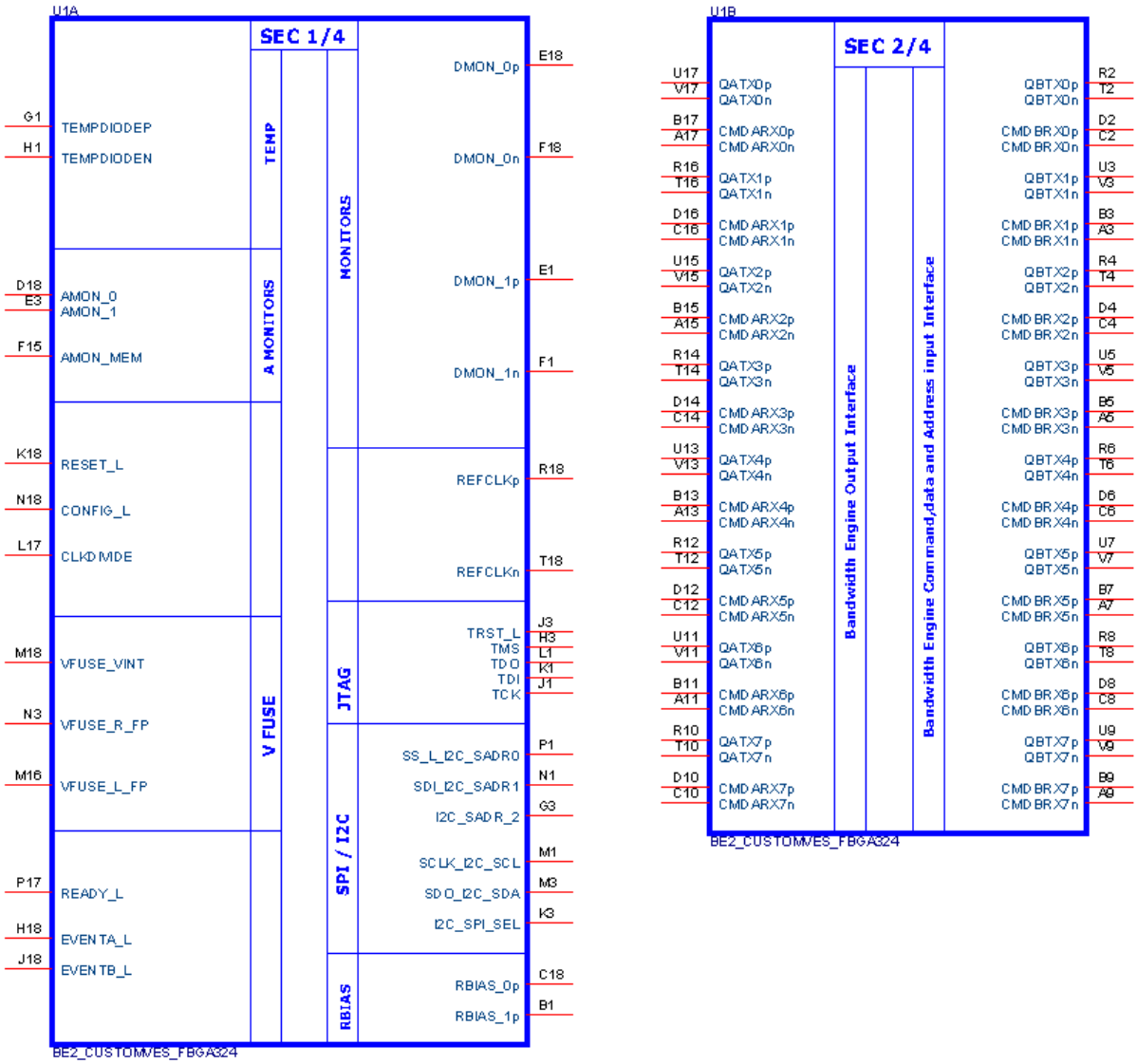
# Heatsink Guidelines

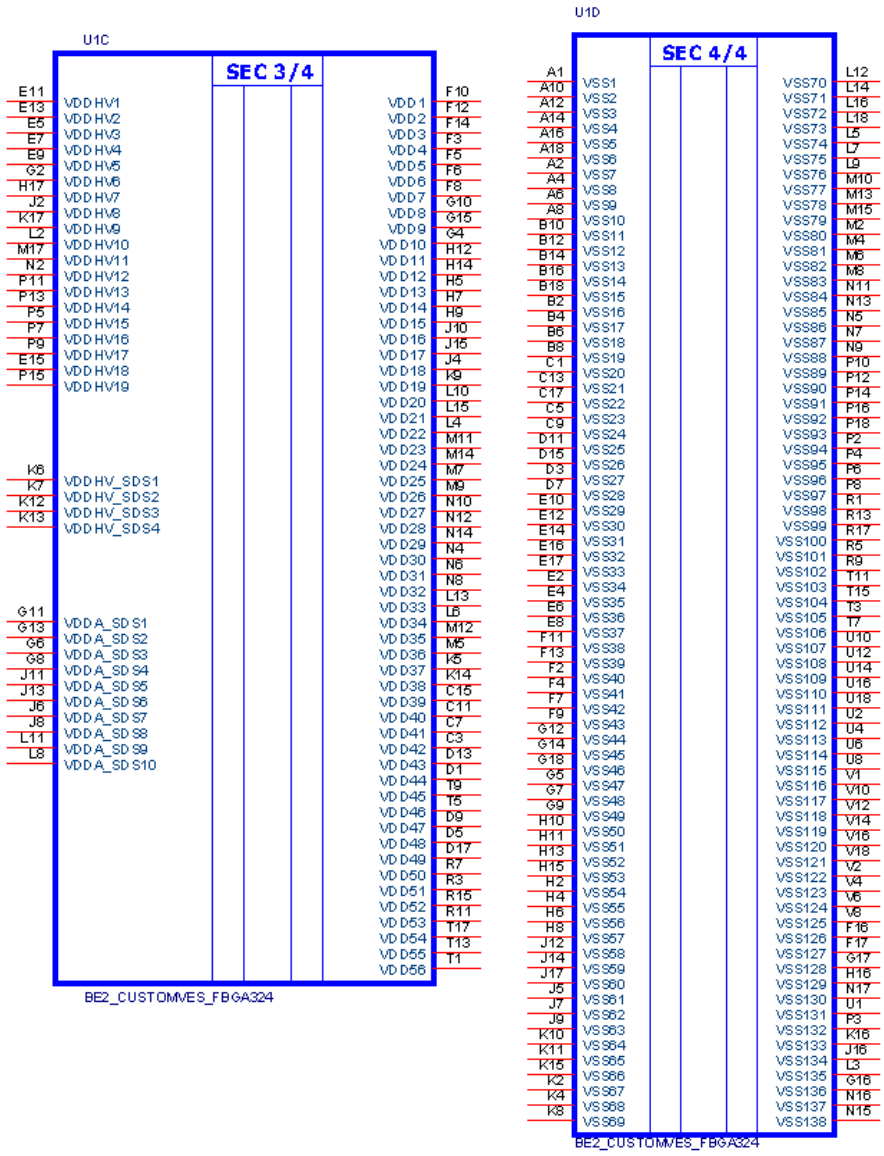
A heatsink is recommended for the Bandwidth Engine 2 device which comes in a lidless flip-chip BGA package. The selected heatsink needs to ensure that the maximum operating case temperature as specified in the device datasheet is not exceeded. Additional information on Thermal Interface Materials, heatsink attachment/removal methods, and allowable Z axis pressure is specified in the device datasheet.

# Schematic Symbol

MoSys provides a schematic symbol (Figure 14) of the BE-2 device that can be used in customer board schematics. The schematic symbol is available in the industry standard ORCAD format as well as in other formats. Please contact MoSys to get the schematic symbol with the format required. Use of the MoSys schematic symbol is recommended as it has been verified.

**Figure 14 Bandwidth Engine 2 Schematic Symbol**






# References

[1] DS-602 Bandwidth Engine 2 Family MSR620 Datasheet
DS-603 Bandwidth Engine 2 Family MSR720 Datasheet
DS-604 Bandwidth Engine 2 Family MSR820 Datasheet

[2] AN-607, Bandwidth Engine 2 Board Layout Guidelines

[3] AN-609, Bandwidth Engine 2 Power-up and Reset

[4] SP-606 GigaChip Interface Specification --- Version 1.1, Jul. 2014

[5] ER-601 Bandwidth Engine 2 Errata List

# Version History

| Date | Version | Changes |
|---|---|---|
| July 2014 | 0.1 | Initial release. |

7/24/14

MoSys, Inc.
2309 Bering Drive
San Jose, CA
95131 USA

Phone 408-418-7500
Fax 408-418-7501
Web http://www.mosys.com