Bandwidth Engine® Power-Up and Reset

Application Note AN-604

Version 0.1, July 2011
MoSys, Inc.

Power-up

Integrating the Bandwidth Engine device into a system design requires adherence to the power-up, reset, and power down specifications described here.

Power Supply Sequencing and Ramp-up

Before initiating power-up, RESET# must be set Low and held Low. The three power supplies, VDDH, VDD, and VDDA, are allowed to have different slew rates and settling times, however the delay t_{DELAY} between any two supplies reaching their final values must not exceed 100 ms. Table 1 shows the timing and voltage specifications for the supplies. Power-up is also shown in the timing diagram in Figure 1.

Table 1 Supply voltage ramp-up requirements

Power Supply	t_{RISE} (ms)		t_{DELAY}(ms)	Supply Voltage (V)		
	min	max	max	min	nom	max
VDDH	0.1	100	100	1.425	1.5	1.575
VDD	0.1	100	100	0.95	1.0	1.05
VDDA	0.1	100	100	1.045	1.1	1.155

Once the power supplies are stable, the part begins the four phase reset sequence shown in Figure 1 and described in the following section.

Reset

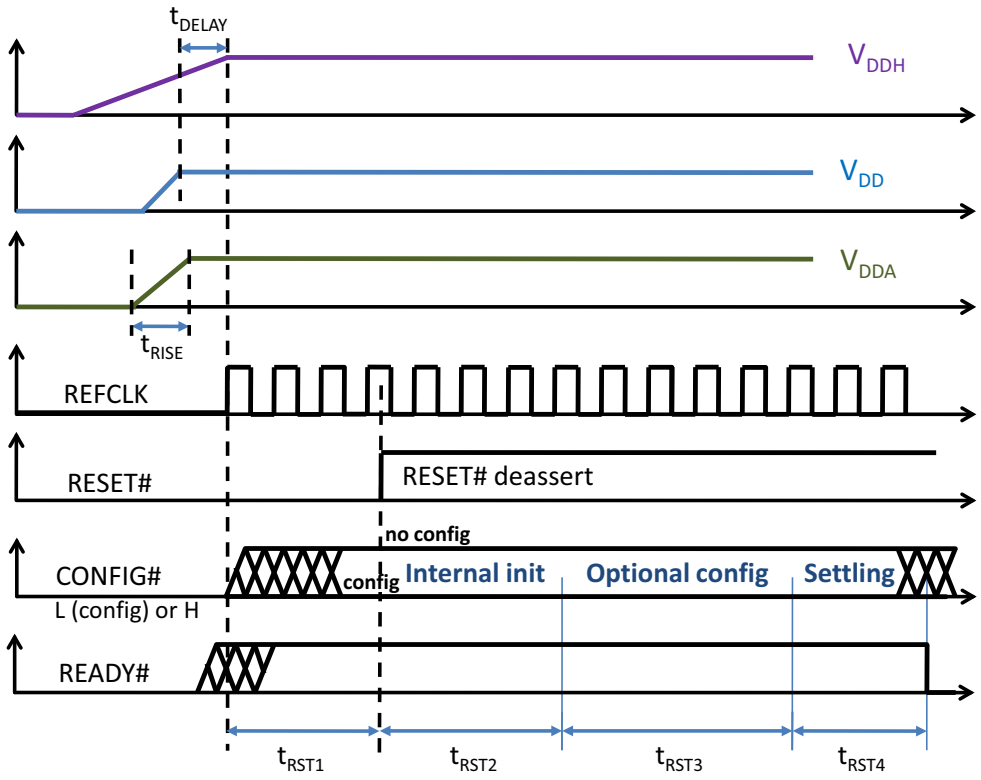
Phase 1

With the power supplies stable, RESET# must remain Low with REFCLK running to allow the clocks to propagate throughout the chip and put it in a known state. Selection of the CONFIG# level must occur while RESET# remains Low, as shown in Figure 1. (To enable the optional configuration phase, set CONFIG# Low. To select the default configuration, set CONFIG# High.) Anytime after the CONFIG# level is valid and the minimum time for t_{RST1} has elapsed, RESET# can be deasserted (set High), marking the end of phase one of the reset cycle. Specifications for RESET# rise time t_R and the delay times for each reset phase are listed in Table 2. Note that while the state of READY# is unknown as the chip powers up, it will be High before the end of phase 1.

Phase 2

Once RESET# goes High, the part enters the second phase of the reset, and completes its internal initialization. At this point the device is ready for the optional third reset phase, configuration. The controller should allow for the maximum t_{RST2} delay before proceeding to the optional configuration.

Figure 1 Power-up reset timing diagram



Phase 3 (Optional)

The elapsed time t_{RST3} for phase three is zero if CONFIG# is High. Otherwise, configuration is controlled through the SPI/JTAG interface, and configuration complete is signaled to Bandwidth Engine through commands in SPI/JTAG.

Table 2 Reset timing parameters

Time	Min	Max	Units	Comment	Notes
t_R (RESET#)	-	20	ns	Use de-bounce circuit for manual reset	1,2
t_{RST1}	0.001	-	ms	Time for clocks to propagate	
t_{RST2}	-	50	ms	Internal initialization	
t_{RST3}	0	-	ms	Zero if CONFIG# is High	3
t_{RST4}	-	12	ms	PLL locking	

1. See “Manual Reset” on page 3 for an example circuit.
2. CONFIG# must be set before RESET# goes high and must not change state before the part is in t_{RST4}.
3. Configuration complete is signaled through commands in SPI/JTAG.

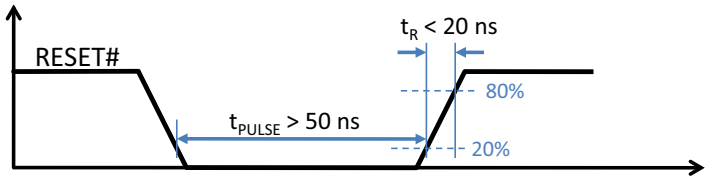
Phase 4

Once the optional configuration is complete, phase four, with duration t_{RST4}, allows for PLL locking. READY# returns Low at the end of this final reset phase to indicate that Bandwidth Engine is ready to process data.

Warm Reset

In addition to the Power-up reset, Bandwidth Engine can be reset at any time while power is on by pulling RESET# low. RESET# must remain low for a minimum of 50 ns as shown in Figure 2 to initiate a reset. Set CONFIG# to the appropriate state while RESET# is Low, and then follow the timing depicted in Figure 1 for t_{RST2}, t_{RST3}, and t_{RST4}.

Figure 2 Warm reset pulse timing



Timing specifications for the warm reset are listed in Table 3.

Table 3 Warm reset timing

Time	Min	Max	Comment
Rise time (20-80%)	-	20 ns	Use de-bounce circuit for manual reset
Active Low time	50 ns	-	No upper limit

Power Down

To power down the chip, pull RESET# Low before turning off the power. Ramp specifications are given in Table 4.

Table 4 Power down requirements

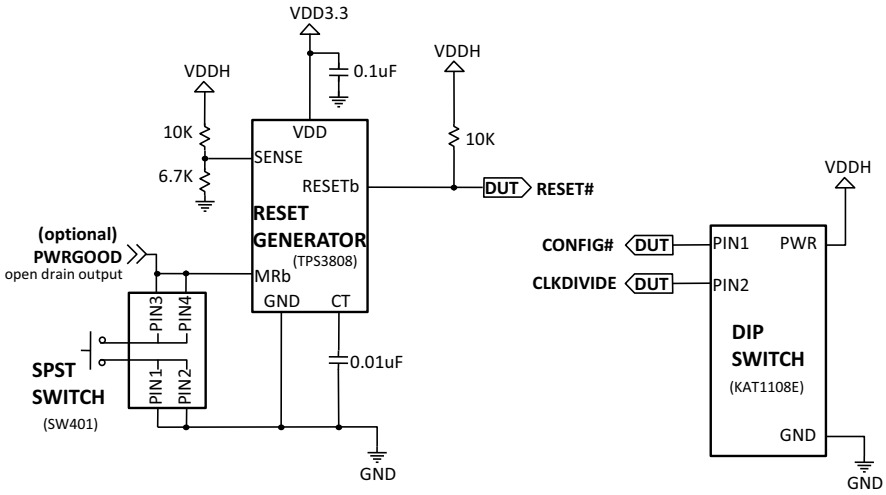
Signal/ Power Supply	t_{FALL}		Units	t_{DELAY} (ms)
	min	max		max
RESET#	-	20	ns	-
VDDH	0.1	100	ms	100
VDD	0.1	100	ms	100
VDDA	0.1	100	ms	100

Manual Reset

If a manual reset option is desired for characterization or debugging, the following circuit generates an appropriate delay to ensure that RESET# stays Low during power-up. This

particular circuit assumes all three supplies come up together within about 50 ms since it monitors just one of the supplies (VDDH) unless the optional PWRGOOD input is used. Depending on the power-up sequence in a system, the 0.01 µF capacitor value may need to be adjusted to ensure that RESET# goes high after the last supply is up and stable.The DIP switch is included to allow CLKDIVIDE and CONFIG# to also be set manually if desired.

Figure 3 Manual reset circuit diagram



Version History

Date	Version	Changes
July 2011	0.1	Initial release.

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