IBIS-AMI Modeling of Bandwidth Engine® Serial Links

Application Note AN-600

Version 0.2, Jan 2013
MoSys, Inc.

Introduction

Historically, HSPICE and MATLAB have been the main tools for modeling high-speed serial links. A new method uses IBIS-AMI (Algorithmic Modeling Interface) models to accurately simulate analog and digital components much faster than traditional SPICE analysis.

This method builds on the existing IBIS methodology to model the blocks within a SerDes unit, such as clock and data recovery (CDR), continuous time linear equalizer (CTLE), and decision feedback equalizer (DFE). It has the additional advantages of IP protection, interoperability, and portability across simulation platforms.

MoSys®, Inc. provides IBIS-AMI models for its Bandwidth Engine MSR576 device. These models are consistent with industry standards and compliant with version 5.0 of IBIS with AMI extensions. The models enable quicker tuning of component parameters and optimization of the board interconnect. However, the models provide only an engineering approximation of actual system behavior. In their present form, they have an accuracy of ±15%. For greater accuracy, MoSys recommends that you use HSPICE modeling.

This document explains the usage of the MoSys IBIS-AMI models. The document contains model descriptions in the main text, followed by example usage in "Appendix A: IBIS-AMI Usage Basics" on page 16.
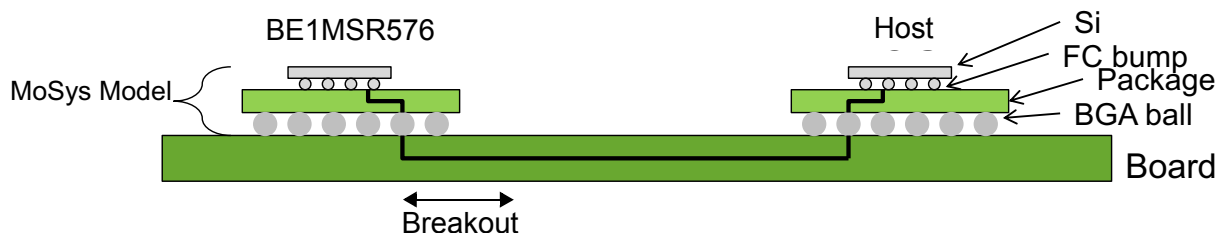
Definitions

Figure 1 Component overview

Table 1 Terminology

Term	Description
Bandwidth Engine (BE1)	The MoSys™ device which is also known as MSR576.
BER	Bit Error Rate
BGA (Ball Grid Array)	The solder ball connecting the package to the board.

Table 1 Terminology *(continued)*

Term	Description
Cursor	Transmitter main coefficient
DOE	Design of Experiments
EH	Eye height
EW	Eye width
Flip Chip (FC or C4)	The bump connecting the chip to the package.
Gain	Receiver (CTLE) gain
Host	The ASIC, ASSP, or FPGA connecting to BE.
MoSys Package Model	This will include the TX and RX package. It represents the model from flip chip to the BGA/board interface. It includes the BGA, but not the BGA pad on the board.
mv	millivolt (10^{-3} volts)
Pole	Receiver (CTLE) pole
Post	Transmitter one delayed from cursor coefficient
Pre	Transmitter one ealier than cursor coefficient
ps	picosecond (10^{-12} seconds)
RX	Receiver
TDR	Time Domain Reflectometry
TDT	Time Domain Transmissometry
TX	Transmitter
Zero	Receiver (CTLE) zero

Supported Simulation Tools

One key advantage of IBIS-AMI is that it allows interoperability across multiple simulation platforms. MoSys's IBIS-AMI models can be incorporated into any simulation tool which supports IBIS-AMI v5.0. This application note will primarily focus on using IBIS-AMI models with Agilent's ADS simulation tool, v2011.

IBIS-AMI Files

An IBIS-AMI suite consists of three main files (.ibs, .ami, .dll) which are listed in Table 2.

Table 2 IBIS-AMI Files

File	Description
.IBS	Analog description of the I/O buffer in V/T and V/I curve format.
.AMI	Parameter information, which is passed to the simulator.
.DLL	Executable code, which contains compiled IP information.

MoSys currently provides IBIS-AMI models for the Windows platform only. Models for the Linux platforms will be provided at a later date.

Design Kit

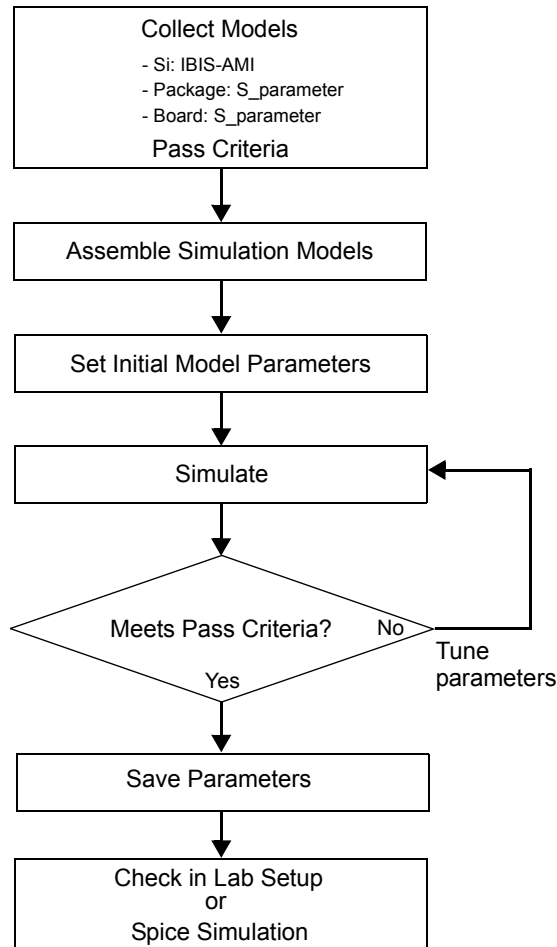The design kit consists of the following files:

• IBIS-AMI files

• MoSys Package models

- Two example board channel files
- Example simulation file (for Agilent ADS). Usage is shown in "Appendix A: IBIS-AMI Usage Basics" on page 16.

System and Model Overview

Figure 2 shows an example IBIS-AMI model setup and simulation procedure.
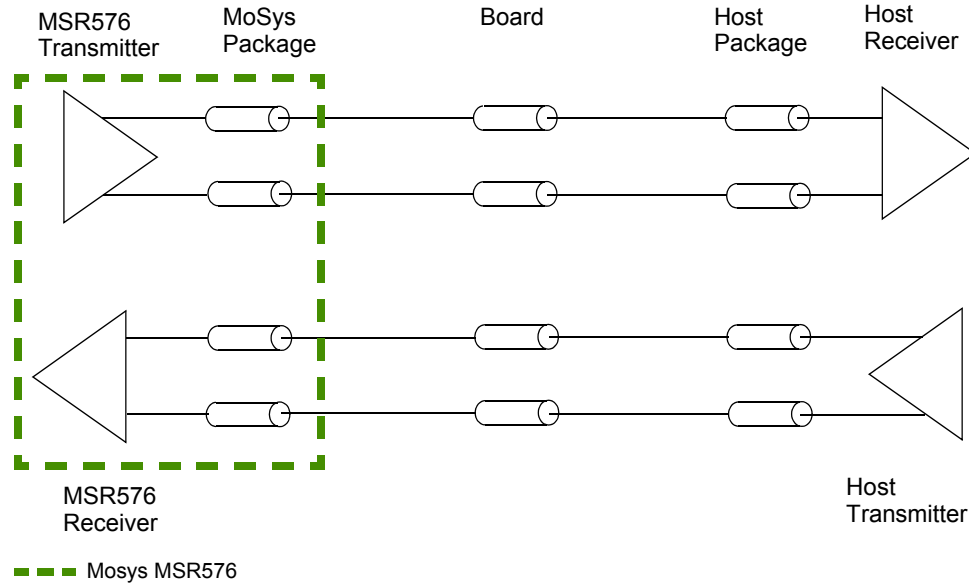
Figure 2 IBIS-AMI setup and simulation procedure

```
          Collect Models
          - Si: IBIS-AMI
          - Package: S_parameter
          - Board: S_parameter
          Pass Criteria
                |
         Assemble Simulation Models
                |
         Set Initial Model Parameters
                |
            Simulate  <----------+
                |                 |
         Meets Pass Criteria? --No--> Tune
                |                      parameters
               Yes
                |
          Save Parameters
                |
         Check in Lab Setup
               or
         Spice Simulation
```

A high-speed design using IBIS-AMI models generally includes the following blocks:

- Transmitter
  - IBIS-AMI model
  - Transmitter pad capacitance
  - Transmit package
- Board channel model
- Receiver
  - Receiver (IBIS-AMI based)
  - Receiver termination and pad capacitance
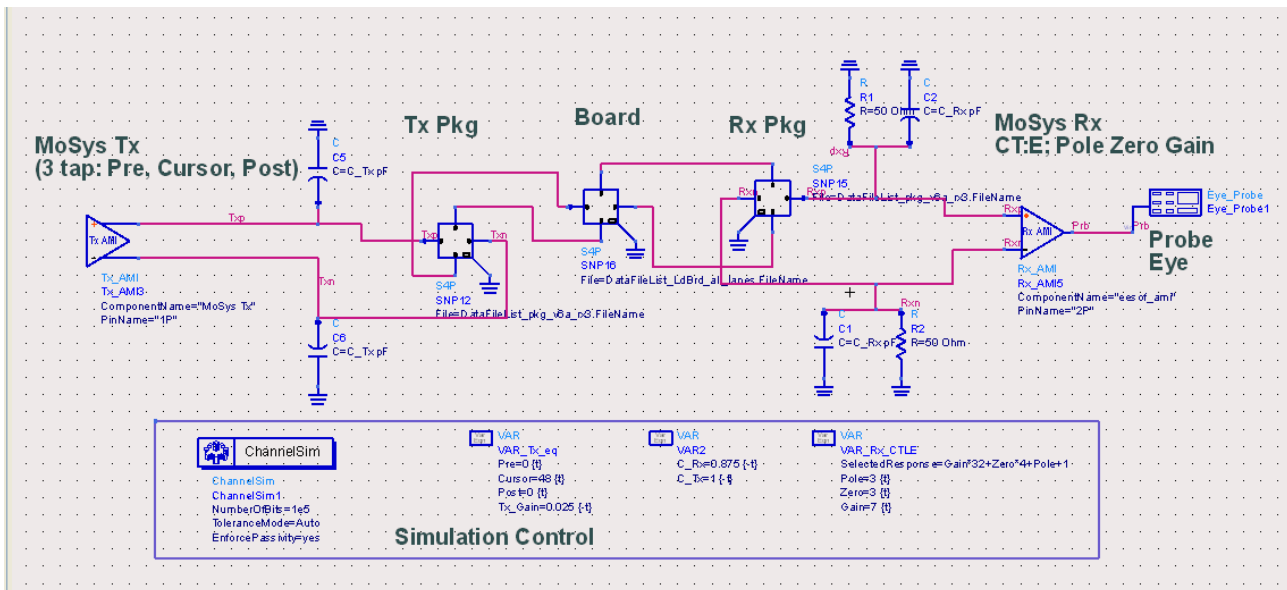
– Receiver package

An example IBIS-AMI setup is shown in Figure 3.

Figure 3 IBIS-AMI model setup overview

Figure 3 IBIS-AMI model setup overview

An schematic example of the IBIS-AMI setup is shown in Figure 4.

Figure 4 High-speed link model details incorporating IBIS-AMI transmitter and receiver models.

An example IBIS-AMI setup and simulation procedure is shown in Figure 2. Note that explicit TX, RX capacitance, and RX termination instances are required in the MoSys model.

Transmitter and receiver pad capacitance parameters and default parameters are shown in the following table.

Table 3 Transmitter and receiver capacitance for MSR576

Parameter	Default Value (pF)	Description
C_Tx	1.0	Transmitter pad capacitance
C_Rx	0.875	Receiver pad capacitance

Transmitter Model

The transmitter in the MSR576 device includes a three-tap pre-emphasis circuit, with pre-cursor, main cursor, and post-cursor taps, as shown in Figure 5.

The Pre-cursor and Post-cursor control the amount of pre-emphasis that is applied to the transmitted signal. The minimum, maximum, and default values for the Pre, Cursor, and Post parameters in the AMI model are shown in Table 4. All the parameters have an integer step size of 1, which corresponds to a voltage increment of V_{BO} = 17.08 mV. The Cursor parameter ranges from 17 to 48. This is primary control for the transmitter swing. Together with the Pre and Post taps, the transmitter equalization can be controlled.

The default value for the Pre and Post parameters is 0, which means that no pre-emphasis is applied to the transmitted signal. Setting the Pre and Post parameters to their minimum values (-8 and -16, respectively) applies the maximum amount of pre-emphasis to the transmitted signal. By lowering the cursor amplitude, the equalization levels can be increased.

Figure 5 A simplified transmitter FIR filter (upper left), schematic view (right), and resulting example bit stream (lower left).
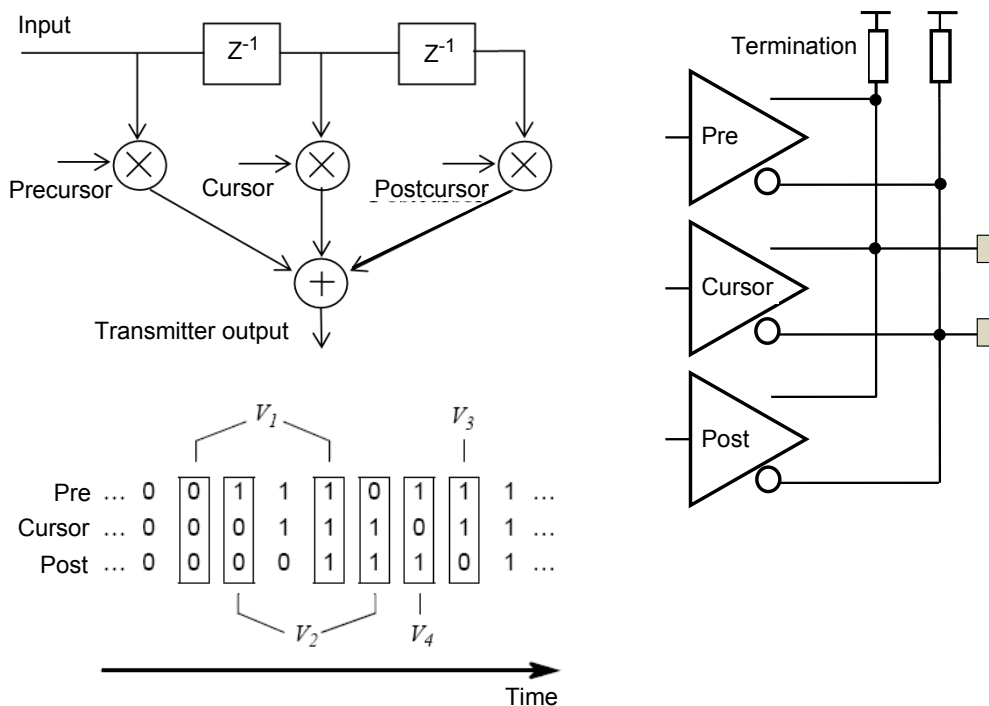
Table 4 Transmitter parameters in IBIS-AMI model.

Parameter	Max	Min	Default	Register	Comment
Pre	-8	0	0		-8 is maximum equalization
Cursor	48	17	48		48 is maximum swing
Post	-16	0	0		-16 is maximum equalization

The differential output voltage is a linear combination of the pre-cursor, cursor, and post-cursor bit values, weighted by tap weights. For example, consider a bit stream consisting of a long series of 0s, then 1110, then a long series of 1s. Figure 5 is a snapshot of the pre-cursor, cursor, and post-cursor bit streams. It labels some combinations of bit values by their differential voltage.

The pre-emphasis circuit can produce four possible differential output voltages:

- V_1 occurs when the values of the pre-cursor, cursor, and post-cursor bits are all the same. One sees this voltage when the transmitter sends a steady stream of all 0s or all 1s.

- V_2 occurs when the bit value of the pre-cursor is different from the cursor and post-cursor bit values.

- V_3 occurs when the bit value of the post-cursor is different from the pre-cursor and cursor bit values.

- V_4 occurs when the bit value of the cursor is different from the pre-cursor and post-cursor bit values.

The following formulas show how to compute the four possible differential output voltages.

$V_1 = V_{BO} \times (\text{Cursor} - |\text{Pre}| - |\text{Post}|)$

$V_2 = V_{BO} \times (\text{Cursor} + |\text{Pre}| - |\text{Post}|)$

$V_3 = V_{BO} \times (\text{Cursor} - |\text{Pre}| + |\text{Post}|)$

$V_4 = V_{BO} \times (\text{Cursor} + |\text{Pre}| + |\text{Post}|)$

$V_{BO} = 17.08\text{mV}$

When the transmitter sends a steady stream of all 0s or all 1s, or when pre-emphasis is disabled (Pre = 0, Post = 0), the differential voltage V_1 simply equals 17.08 mV times the AMI Cursor parameter. In these conditions, V_1 ranges from 290 mV (Cursor = 17) to 820 mV (Cursor = 48).

The V_4 combination of bit values (cursor is different from pre-cursor and post-cursor) causes the greatest pre-emphasis relative to the V_1 combination (pre-cursor, cursor, and post-cursor are the same). The following formula gives the maximum preemphasis in dB over all bit values:

Pre-emphasis (dB) = 20 x log (V_4/V_1)

The following table shows the differential output voltages and maximum pre-emphasis that result from several example values of the AMI Pre, Cursor, and Post parameters.

Table 5 Differential output voltage for example values of AMI parameter values

AMI parameters	Integer totals	Differential voltage (mV)	

Table 5 Differential output voltage for example values of AMI parameter values *(continued)*

Pre	Cursor	Post	V_1	V_2	V_3	V_4	V_1	V_2	V_3	V_4	Maximum pre-emphasis (dB)
0	32	0	32	32	32	32	547	547	547	547	0.0
-8	32	0	24	40	24	40	410	683	410	683	4.4
0	32	-16	16	16	48	48	273	273	820	820	9.5
-8	32	-16	8	24	40	56	137	410	683	956	16.9
0	36	-8	28	28	44	44	478	478	752	752	3.9
-4	48	-8	36	44	52	60	615	752	888	1025	4.4
-8	48	-16	24	40	56	72	410	683	956	1230	9.5

Transmit Jitter

Based on silicon results, MoSys has set the intrinsic jitter of the transmit buffer in the IBISAMI model to:

• Random Jitter (RJ): 800 fs (rms)

• Deterministic Jitter (DJ): 12 ps (p-p)

These jitter numbers represent the worst case jitter across process, voltage, and temperature (PVT). They are built into the IBIS-AMI model. Any additional jitter due to the data pattern (pattern-dependent jitter) or the channel (for example, ISI) will be added by the simulation tool.

Package Models

The IBIS-AMI model describes the silicon chip, but not the package. MoSys provides 4-port S-parameter models in Touchstone format (.s4p suffix) for the Bandwidth Engine package. There is one model that represents a transmit pair, and another model that represents a receive pair. You must insert the appropriate package model between the IBIS-AMI model and the channel model. Figure 6 and Figure 7 show how the four ports of the package TX/RX models correspond to the P and N ports of the IBIS-AMI and channel models. It is important to follow this port ordering and orientation.

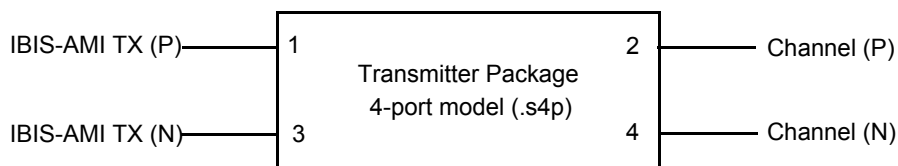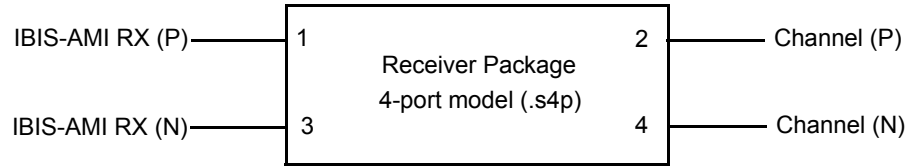**Figure 6** Package model for transmitter. Ports (1,3) need to connect to the SerDes.

Figure 7 Package model for receiver. Ports (1,3) need to connect to the SerDes.

IBIS-AMI RX (P) —— 1   Receiver Package   2 —— Channel (P)

IBIS-AMI RX (N) —— 3   4-port model (.s4p)   4 —— Channel (N)

Channel Models

MoSys provides two sample channel models: a short and a medium loss channel. These are 4-port S-parameter models in Touchstone format (`.s4p` suffix). The insertion and return loss profiles for the channels are shown in Figure 8. At 5.156 GHz (the fundamental frequency when the data rate is 10.3125 Gbps), the channel loss for the short and medium loss models is approximately 2dB and 8dB, respectively. These models can be used as are placeholders during initial setup.

Figure 8 Sample channel models. Either port pair (1,3) or (2,4) can be used for TX or RX.

Channel_in (P) —— 1   Channel   2 —— Channel_out (P)

Channel_in (N) —— 3   4-port model (.s4p)   4 —— Channel_out (N)
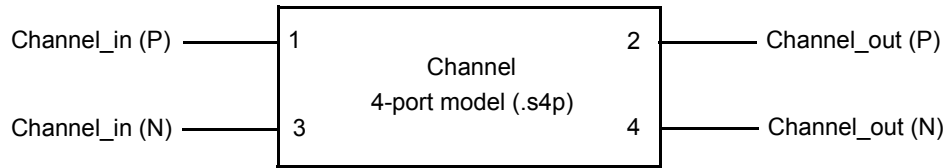
Figure 9 Short channel (2dB) model characteristics, corresponding to a ~2" PCB trace. RL_brd suggests a board return loss limit.
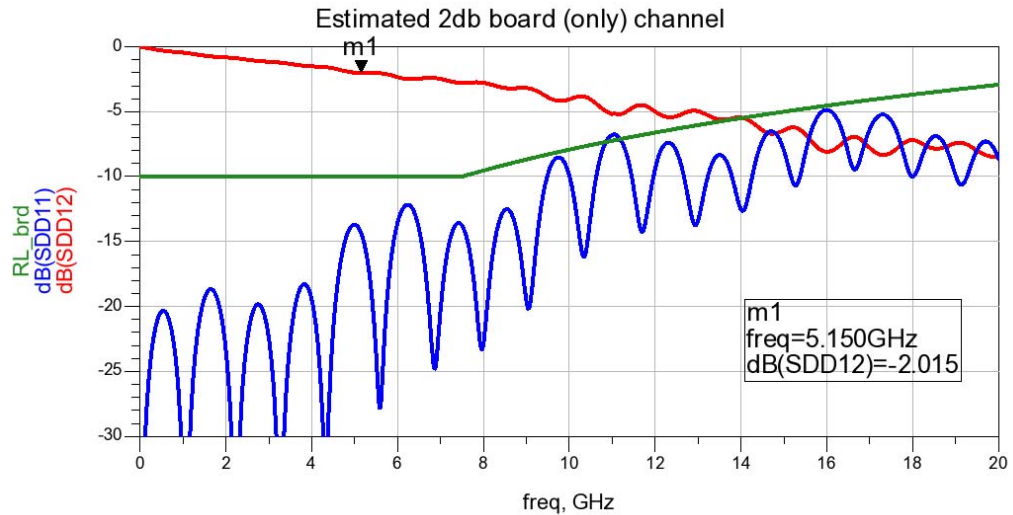
Figure 10 Longer channel (8dB) model characteristics, corresponding to a ~9" PCB trace. RL_brd
suggests a board return loss limit.

Estimated 8db board (only) channel
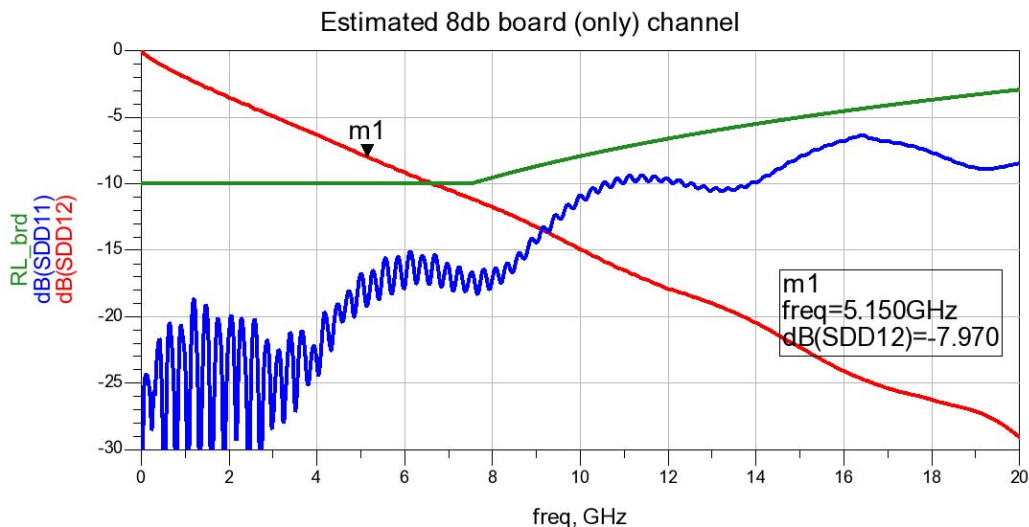
Receiver Model

The receiver in the MSR576 device, shown in Figure 11, consists of the following blocks:

• Receive buffer, which has 50 Ω termination followed by an internal AC coupling

• Continuous-time linear equalizer (CTLE)

• Sampler

Figure 11 MSR576 receiver blocks
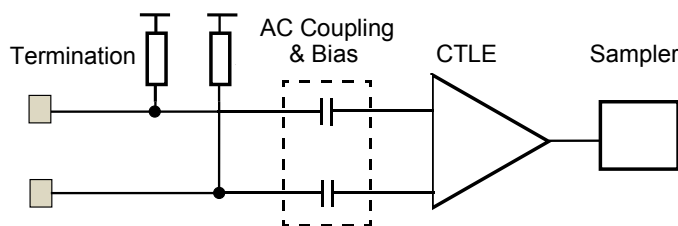
The CTLE block is the only block that one needs to adjust based on channel
characteristics. It provides high-frequency gain to equalize for channel loss. The CTLE
block has three adjustable parameters:

• DC gain

• Zero frequency

• Pole frequency

The zero setting provides "peaking" while the pole pulls down the frequency response.
The minimum, maximum, and default values for the three parameters in the AMI model
are shown in Table 6, and a typical response is shown in Figure 12.

Figure 12 Example CTLE frequency response curve
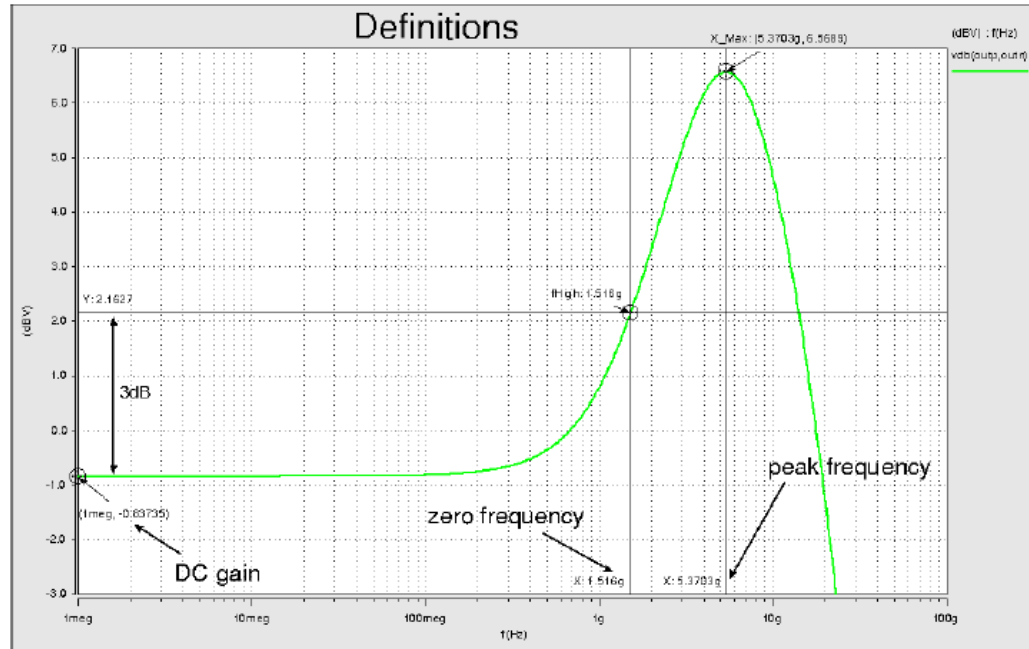
Table 6 CTLE parameters in IBIS-AMI model, and their simplified and approximate range. The actual characteristics are set by the equalizer control and response is coded in the IBIS-AMI model.

Parameter	Min	Max	Default	Unit	Register	Comment
Gain	0	15	4	dB		Changes DC gain by ~12-13 dB. At zero=0 DC gain range (-6 to 7.5 dB), zero=3 DC Gain range (-13 to 1 dB), zero=7 DC Gain range (-20.5 to -7 dB). Reducing DC gain effectively provides more peaking.
Zero	0	7	3	GHz		Changes zero location from 0.7 GHz to 3.9 GHz.
Pole	0	3	3	GHz		It is recommended the Pole setting should not be different from default.

Receiver Jitter

Based on silicon results, MoSys has set the intrinsic jitter of the receive buffer in the IBISAMI model to:

• Random Jitter (RJ): fs (rms)

• Deterministic Jitter (DJ): ps (p-p)

These jitter numbers represent the worst case jitter across process, voltage, and temperature (PVT). They are built into the IBIS-AMI model. Any additional jitter due to the data pattern (pattern-dependent jitter) or the channel (for example, ISI) will be added by the simulation tool.

Simulation and Optimization

Model Setup

The IBIS-AMI model can be assembled using MoSys board and Host models, as shown in Figure 3 and Figure 4.

In addition some model parameters can be set so that they can be tuned. Typically these would be the TX equalization and RX equalization settings.

Additional options allowing multiple interconnect configurations to be swept can also be included. These could include multiple board traces, package traces having different lengths or impedance or other properties.

Crosstalk

The single line model can be extended to include crosstalk. Here the interconnect model includes crosstalk elements. For the model in Figure 13, usually S12P (12 port) or higher port numbers will be required. Adhering to port ordering as described in the interconnect files is essential to capture crosstalk. Here one direction of links is shown, and the other direction model should also be built and analyzed.

Typically the aggressors can be set to be having random data patterns and phase with respect to the victim. It is worthwhile to check for in phase and opposite switching patterns to estimate the worse case scenarios.

Figure 13 Crosstalk setup. Three differential pairs can provide sufficient crosstalk accuracy.
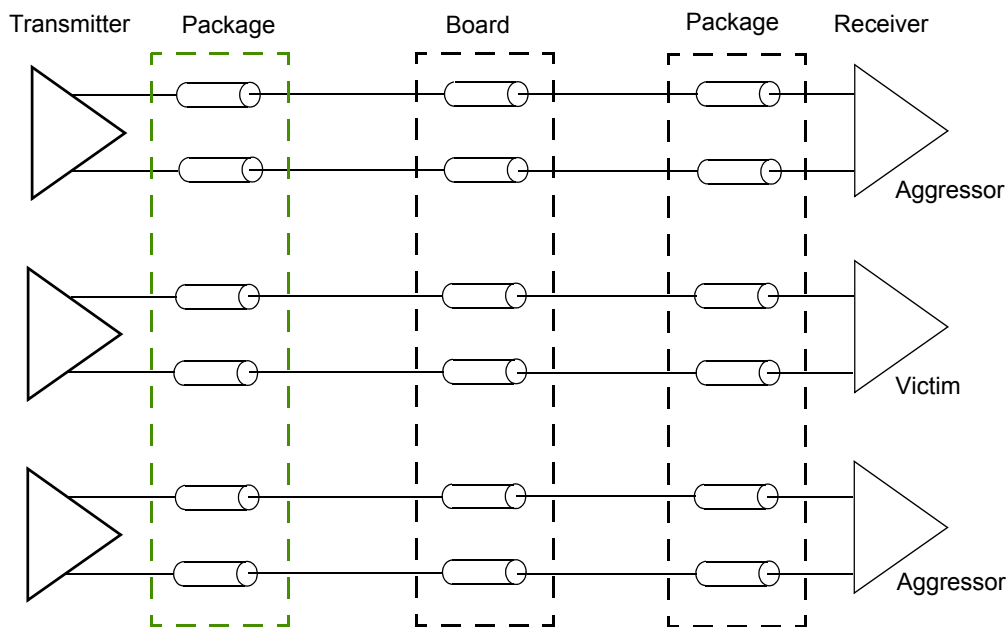
Characterize TX

The characterization setup is shown in Figure 14. Here the AMI Tx is instantiated. A unity gain ideal AMI compliant receiver (a pass-through receiver) is used to receive the signal. Typically the pass-through receiver is available from the simulator vendor (an example is

provided in "Appendix A: IBIS-AMI Usage Basics" on page 16). This setup can help characterize the swing, equalization, and jitter levels. In case of simulation setup, tool, or compatibility issues, this is a good debug and troubleshooting setup as well.

**Figure 14**   TX characterization schematic

MSR576
Transmitter

Channel
(as required)

Probe

Termination

Pass-through Receiver
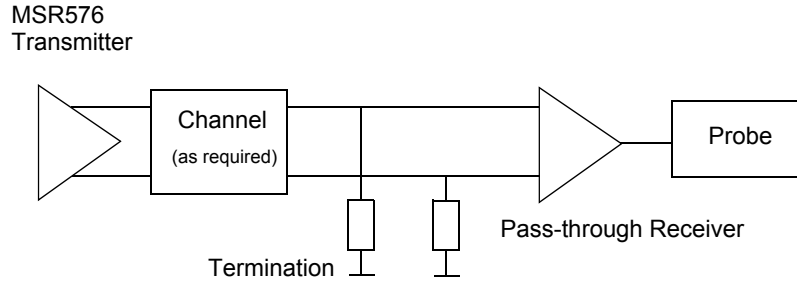
Characterize RX

The receiver can be characterized using the setup in Figure 15. An input step is applied, and the resulting output step response of the receiver can be observed at the output.

This setup is also a good debug and troubleshooting tool.

Figure 15   RX characterization setup

Feed Through
Transmitter

MSR576
Receiver

Probe

Termination
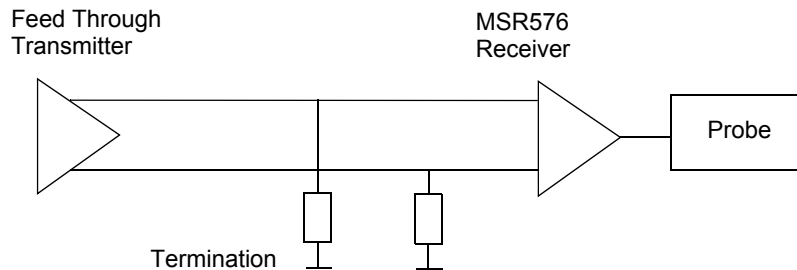
Characterize Interconnect

It is recommended to build an interconnect model, and understand its properties in terms of insertion, return loss, and cross talk in the frequency domain.

It is also desirable to understand those in time domain for discontinuities.

Together, they can be compared with the customer's interconnect acceptance criteria. Typically, for interconnect that is marginal, there may be some iterations required between IBIS-AMI parameter tuning and the interconnect optimization.

Figure 16 S-Parameter characterization of the interconnect for insertion and return loss. Results can be plotted as shown in Figure 10.
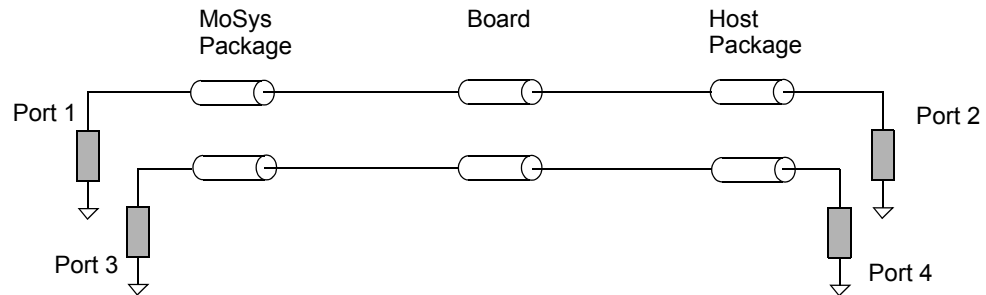
Figure 17 TDR characterization of the interconnect for discontinuities.
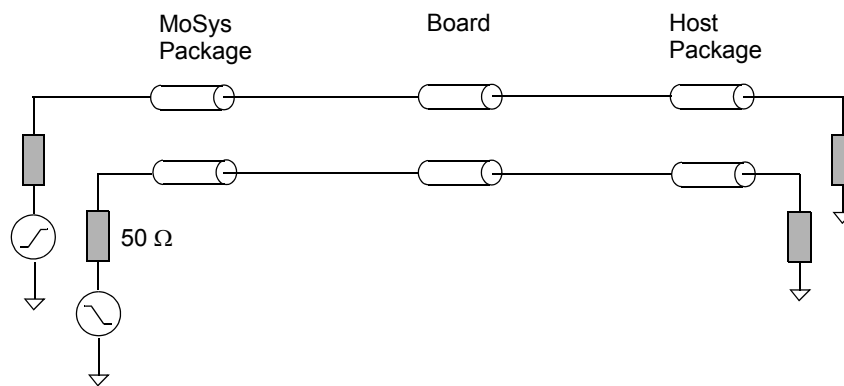
Initial Setting

To aid the user in establishing a quick initial value for the links, Table 7 and Table 8 are provided.

To simplify, it is assumed that both end TX and RX are made of MoSys IP. It is recommended that the user validate these initial settings with the right IBIS-AMI models, and channels, or create an equivalent table.

The user can quickly establish rough channel settings based on the step response. For this, provide one of the following from the transmitter:

• a step (e.g., "00000000001111111111")

• a pulse (e.g., "00000000001000000000")

Observe the step or pulse response at the receiver output. Tune the transmitter and receiver equalization within user intended limits. A good step response will be a resulting sharp step, with minimum of "RC" charge up or ripples. Alternatively, a good pulse response is one where the pre and post cursors are minimized.

Figure 18   Channel characterization setup. Similarly the reverse direction can be set up (i.e., with Host transmitter and MSR576 receiver).
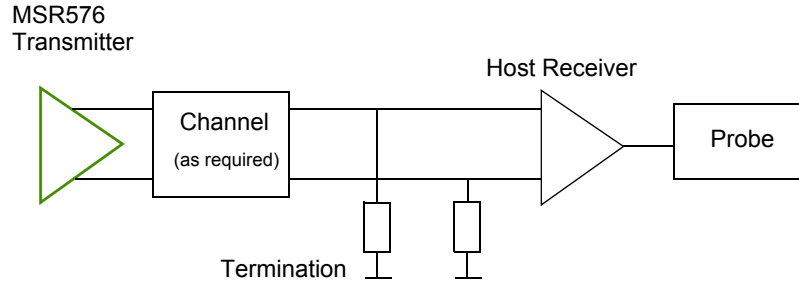
Figure 19   Example of estimating initial equalization using step response (10 Gbps, 1UI=100ps).
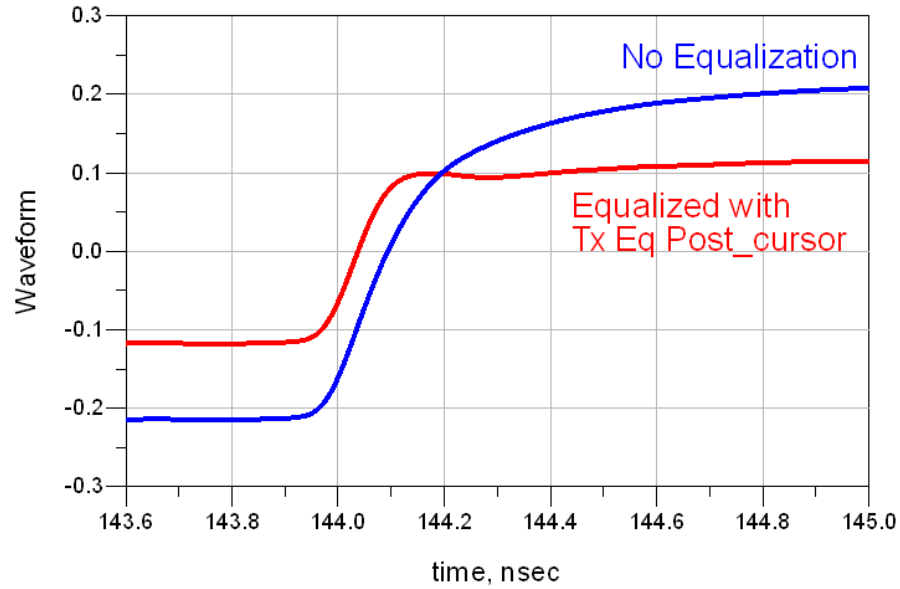
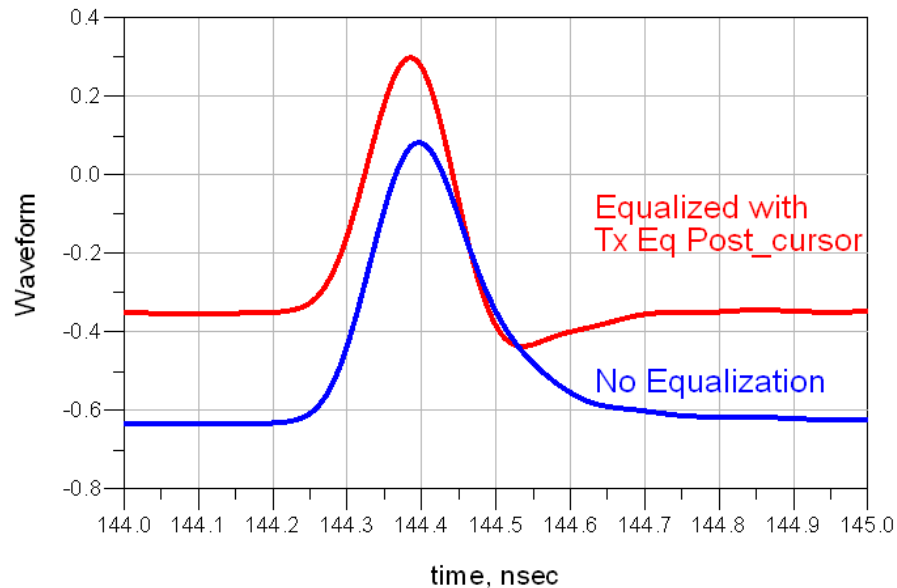**Figure 20**   Example of estimating initial equalization using pulse response (10 Gbps, 1UI=100ps).

Table 7   Initial TX equalization setting

Channel Loss (dB)	Pre	Cursor	Post	Comment
6	-1	42		
8	-2	42	-11	
10	-2	42	-12	
12	-4	40	-14	
14	-4	38	-16	

Table 8   Initial RX equalization settings

Channel Loss (dB)	Pole	Zero	Gain	Comment
6	3	3	14	
8	3	3	9	
10	3	3	7	
12	3	3	7	
14	3	4	7	

Tuning

In general, the initial guess will need to be optimized further to include in factors such as buffer and interconnect variations and jitter. Three methods can be used:

• Interactive tuning — The user tunes parameters, and observes results such as eye height and width interactively.

• Batch tuning — The user simulates relevant parameters (usually around the initial guess), and processes the results later.

• Optimization — Uses goal-seeking algorithms. This is particularly relevant when the number of parameters is large (e.g., TX equalization and RX equalization). However, you should check if a local optimum is not reached.

Examples are provided in Appendix A ("Tuning" on page 23).

Pass Criteria

For the Mosys Receiver, the desired pass criteria is to have an eye width opening of 10 ps and an eye height opening of 50 mV at a BER of 1E-15.

Model Limitations and Future Enhancement

The IBIS-AMI model is a preliminary model that should be used for AC analysis only. It should not be used for DC level settings or compatibility. Planned additional enhancements for the IBIS-AMI model are:

• Model is for Typical conditions only. Other corners will be added.

• DFE to be included in the model.

• Jitter numbers will be improved with Si correlation.

Appendix A: IBIS-AMI Usage Basics

This section provides more detail into the specific schematic and simulation methods using the Agilent ADS simulator. However, these steps can also be mapped to other simulators.

It is highly recommended that the IBIS-AMI simulator vendor website design kits be studied, as they will have detailed tutorials and examples. A basic tutorial is provided here to enable the user to get a quick start using the MoSys models.

Topics covered:

- "General Schematic Setup" on page 17
- "Setting Up the Transmitter Model" on page 18
- "Setting up the Receiver Model" on page 20
- "Simulation Control and Display" on page 22
- "Tuning" on page 23

These are the steps for IBIS-AMI schematic creation, simulation, and display. The following figures show examples of these steps.

1. Schematic creation
- Open ADS schematic window — See Figure 21, "Schematic open," on page 17
- Instantiate the AMI TX and RX and Probe — See Figure 22, "Instantiating AMI elements into the schematic.," on page 17
- Point to right models — See Figure 24, "Setting properties," on page 19
2. Simulation — See Figure 28, "Simulation control," on page 22
- Set up the channel simulation (time)
- Set up the right variables
- Simulate
3. Display results — See Figure 29, "Display results," on page 23

General Schematic Setup

Figure 21   Schematic open

Figure 22   Instantiating AMI elements into the schematic.

Palette (zoomed view)
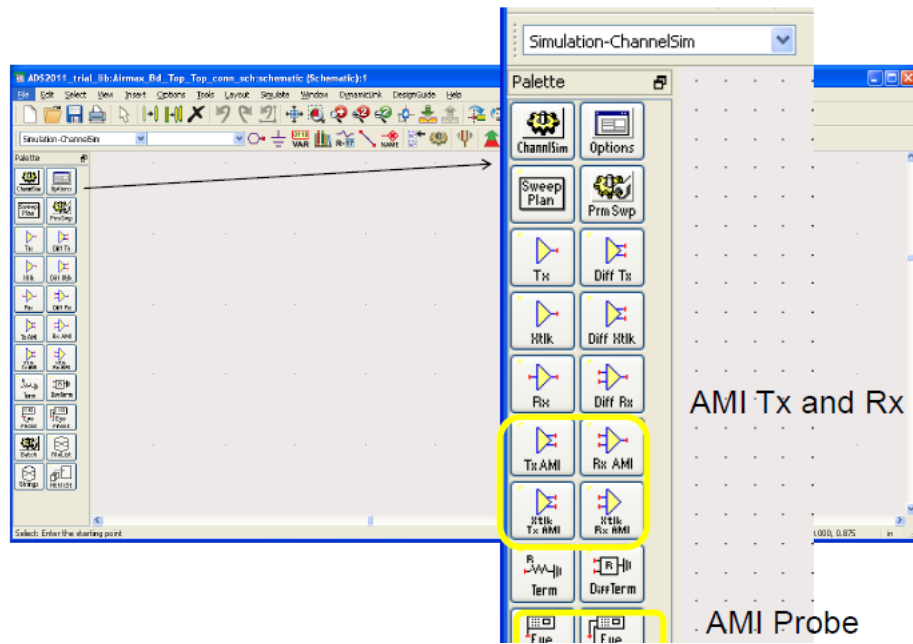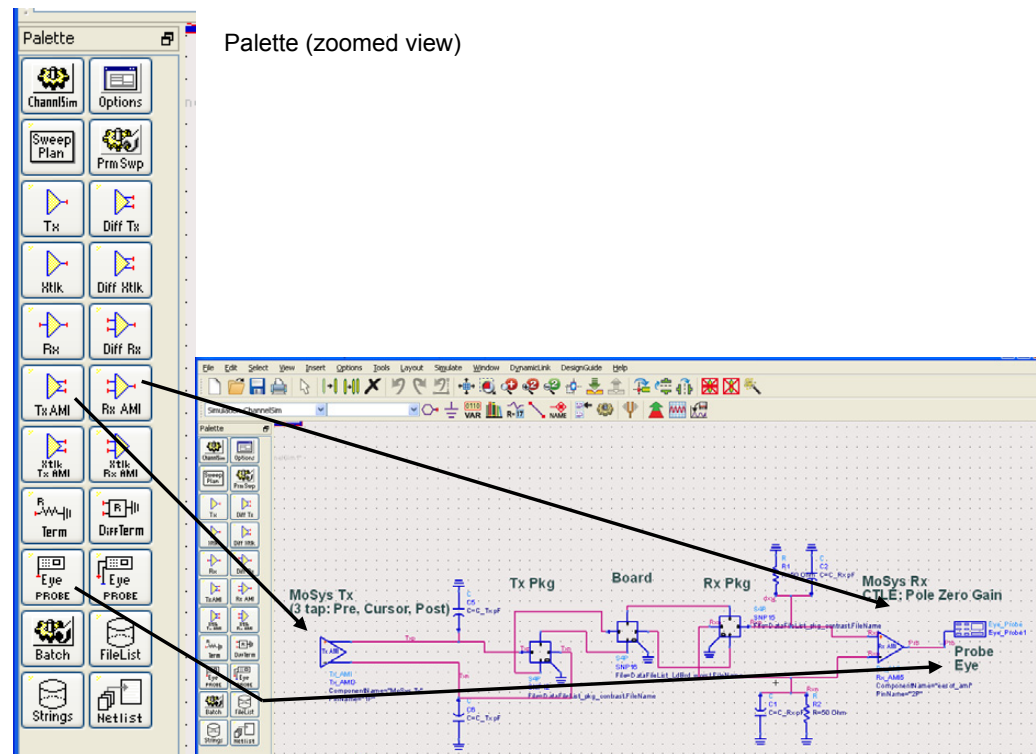
- Double-click on icon, and point to the IBIS models.
- Once the properties are visible, edit properties to desired setting.

Figure 23 Location of some (Agilent ADS) useful components such as transmitter and receiver pass-through, along with some link examples.
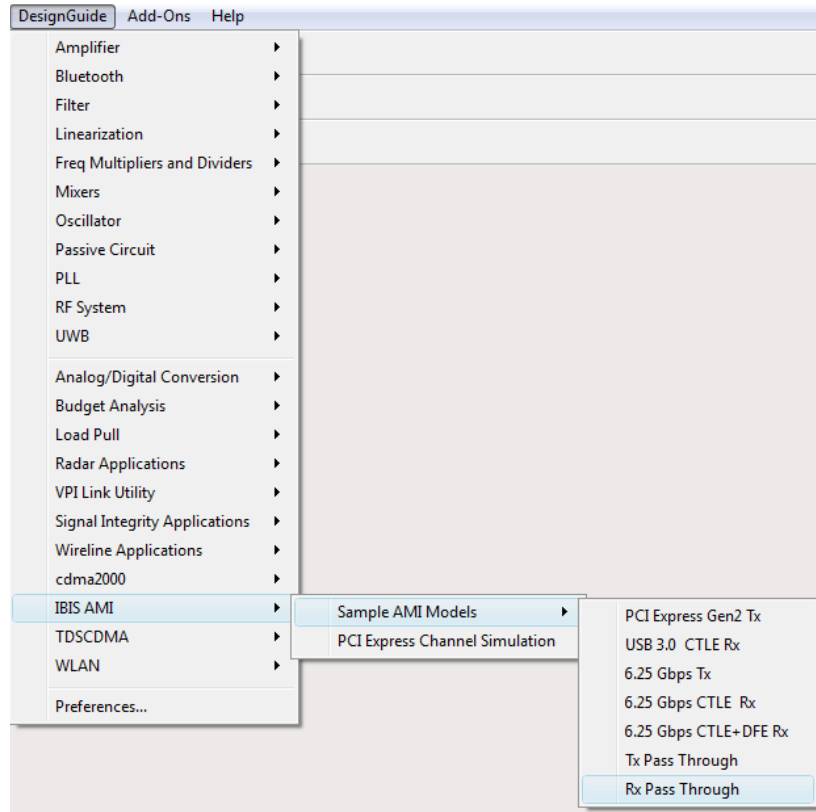
Setting Up the Transmitter Model

The Tx IBIS/Ami model can be directly controlled by changing the tap parameters in the Tx AMI symbol. The coefficient numbers need to be integers, and within the specified range. Alternatively, the equalization and swing can be setup as variables that are easier to control interactively or through simulation sweeps. For example, The Pre, Cursor, and Post parameters can be set in Agilent's ADS simulation tool, v2011.01. Follow these steps:

1. Instantiate a TX AMI model into the schematic. Link it to the TX IBIS file provided by MoSys.

2. Double-click on the transmit model. The following GUI window in Figure 25 should open up.

3. Click on the AMI tab.

4. Click on the first tap (-1), and select "User specified". Type variable "Pre" into the box, as shown in Figure 25. This assigns the "Pre" to -1 tap entry of the model.

5. Click on the second tap (0), and select "User specified". Type "Cursor" into the box.

6. Click on the third tap (1), and select "User specified". Type "Post" into the box.

7. Click "OK" to close the window.

In the top-level ADS schematic, a variable (VAR1) controls the Pre, Cursor, and Post parameters. You can control these settings by changing the variable value.
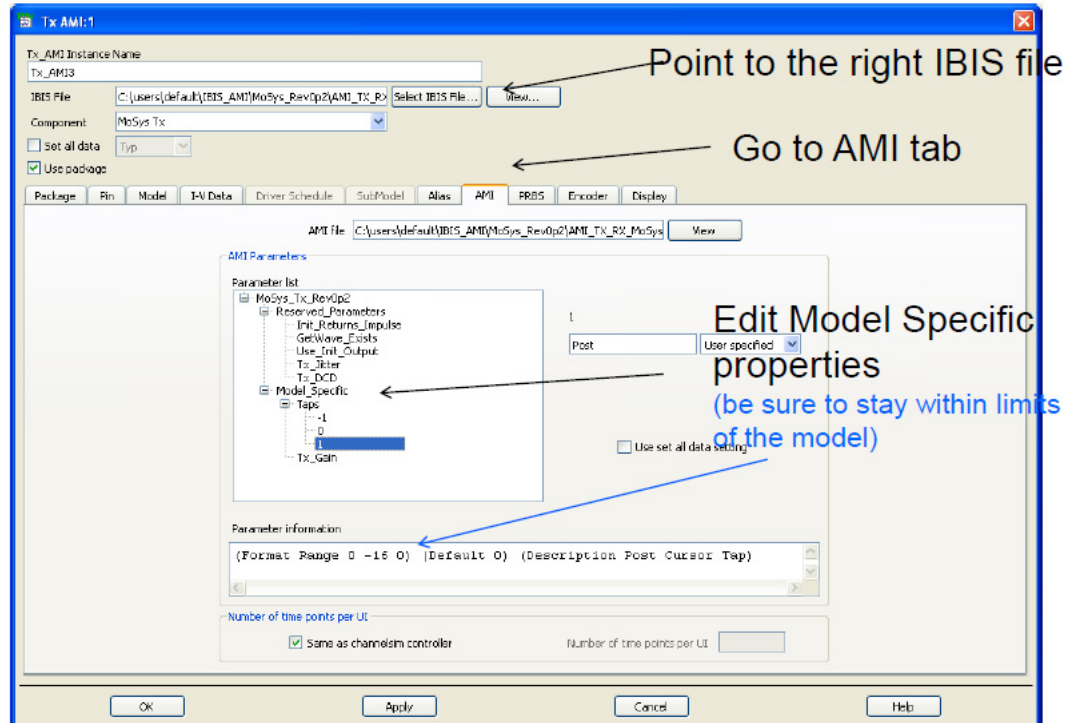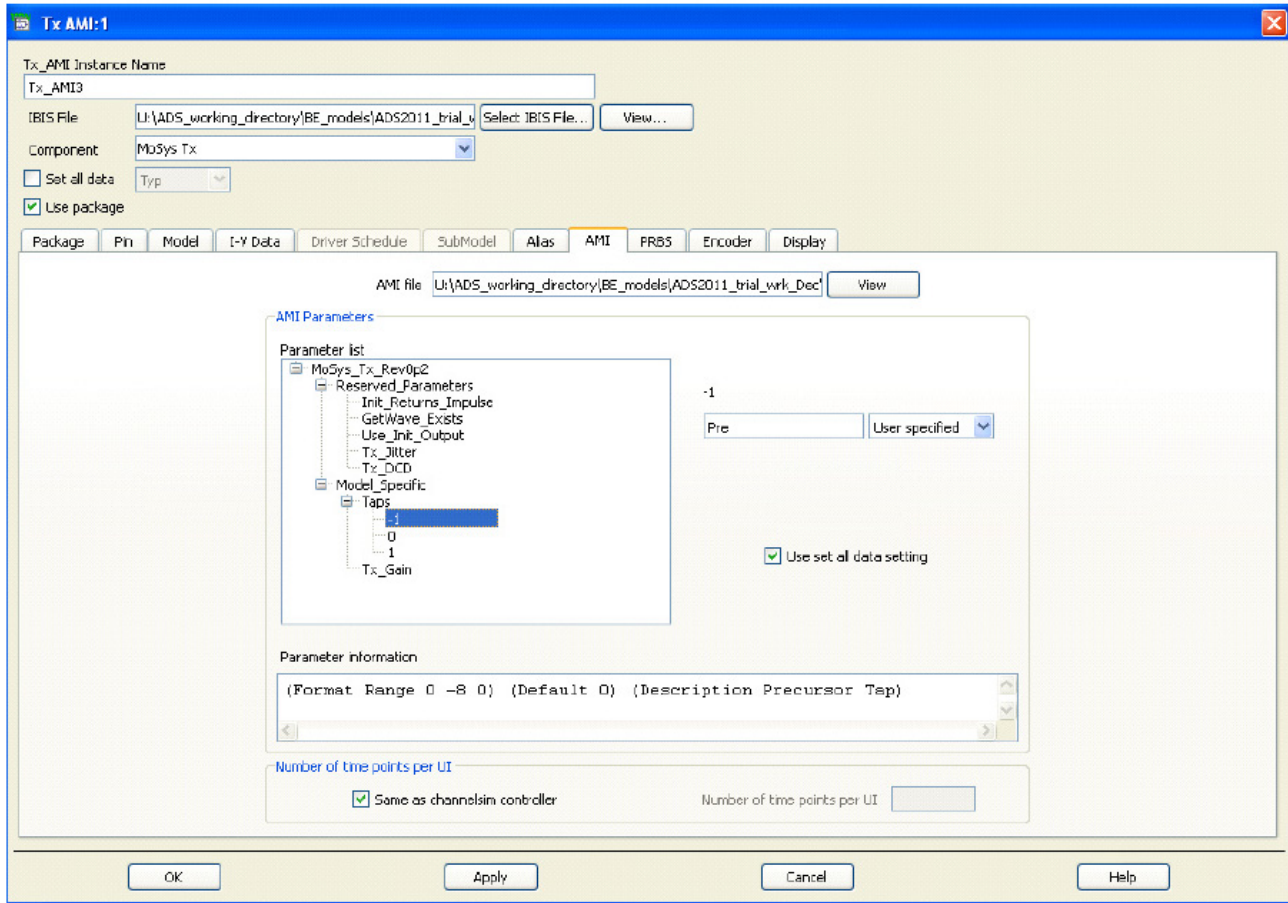
Figure 24 Setting properties

**Figure 25** Transmitter IBIS-AMI window (ADS v2011.01)

Setting up the Receiver Model

The SelectedResponse parameter can be set in Agilent's ADS simulation tool using the following steps:

1. Instantiate an RX AMI model into the schematic. Link it to the RX IBIS file provided by MoSys.

2. Double-click on the receiver model. The GUI window in Figure 26 should open up.

3. Click on the AMI tab.

4. Click on the Model Specific, SelectedResponse, and select "User specified". Type variable "SelectedResponse" into the box as shown in Figure 26. This assigns the "SelectedResponse" variable to the SelectedResponse within the AMI model.

5. Click "OK" to close the window.

In the top-level ADS schematic, a variable (VAR2) controls the SelectedResponse.

Figure 26 Setting SelectedResponse parameter.
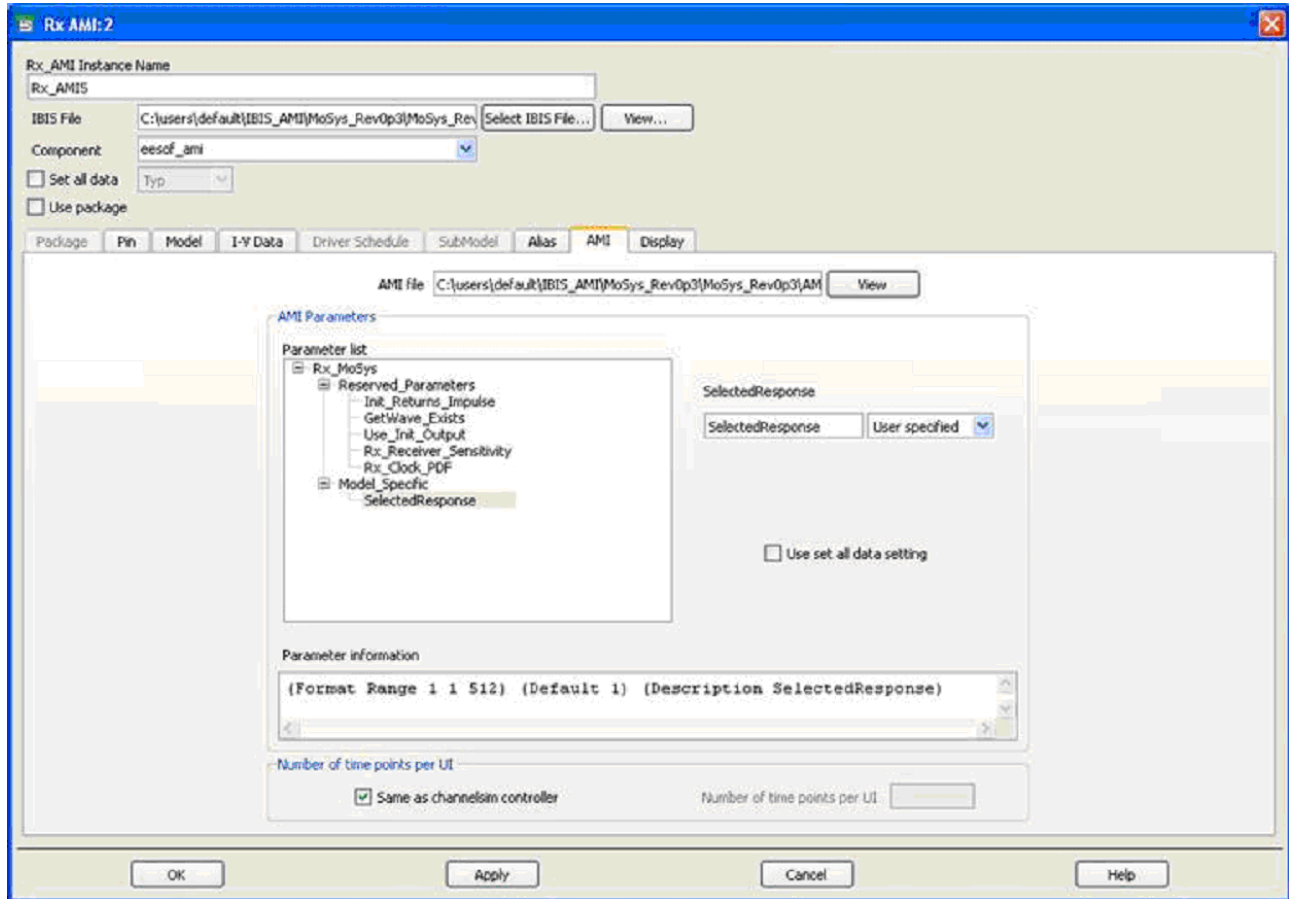
The CTLE response is set by the SelectedResponse parameter. SelectedResponse is a function of Pole, Zero, and Gain. In total, there are 512 responses for all combinations of Pole (8) x Zero (4) x Gain (16) settings at Typical. The equation is shown below.

SelectedResponse = (Gain × 32) + (Zero × 4) + Pole + 1

There are two ways to change SelectedResponse in the Agilent ADS simulation tool:

• By changing it in the top level schematic

• By changing the CTLE parameters in the IBISAMI model for the receiver

The lookup table within the AMI model is arranged into the 512 responses. The user can set the PZG how it looks like in the lane register setting. The SelectedResponse equation translates the PZG settings within the channel simulator, and passing the variable such that the correct response within the model is chosen.

An example is provided in Figure 27.

**Figure 27**   Changing SelectedResponse in the top-level schematic.
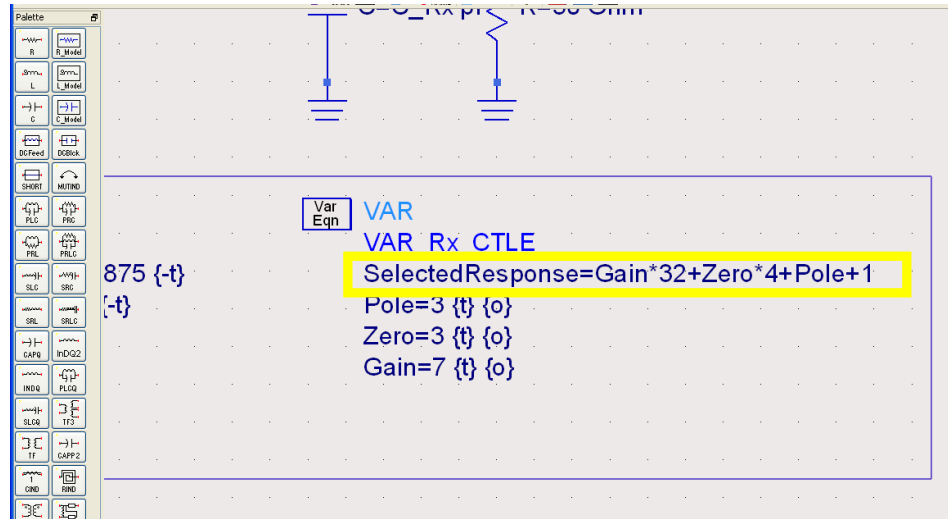
Simulation Control and Display

Figure 28   Simulation control
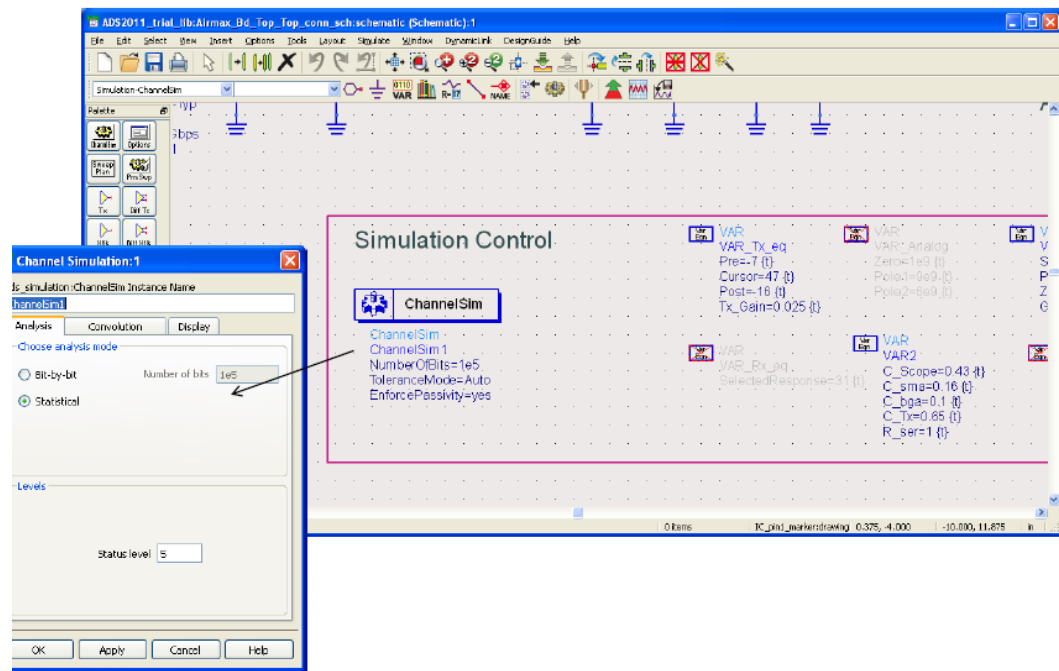
- Two modes are available: Bit-by-bit or statistical.

- To save time, first simulate in bit-by-bit mode, starting with a few hundred bits, then gradually going to a million bits as results confirm expectations. Finally, statistical analysis is desired.

Figure 29 Display results

index	...(Height*3)	...ute(Width)
0.000	0.330	3.055E-11
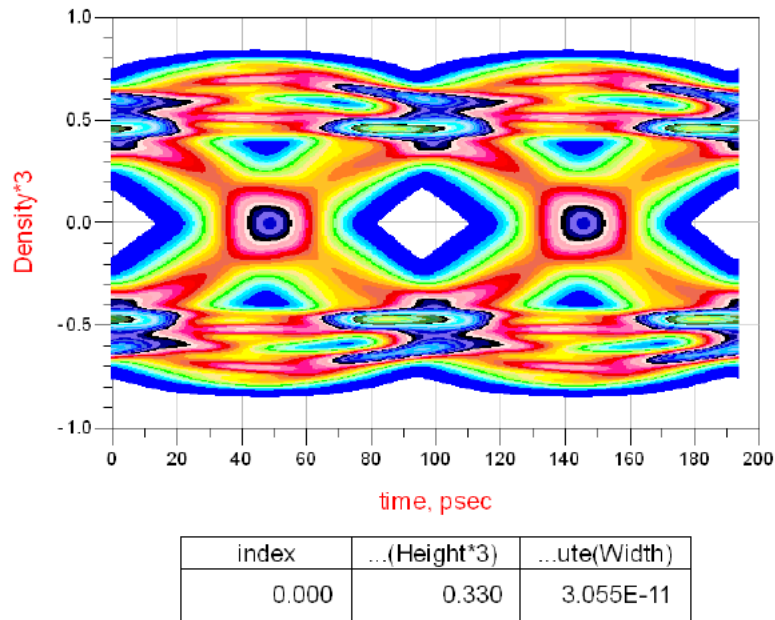
Tuning

Paretto Analysis

It is useful to get a sense of the main system variables. For this, sensitivity analysis can be done such as Paretto or DOE (Design of Experiment). Figure 30 shows an example for Paretto. This analysis shows the sensitivity (loss of eye margin) of the board discontinuity, and sensitivity of the CTLE parameters Pole, Zero, and Gain (PZG).
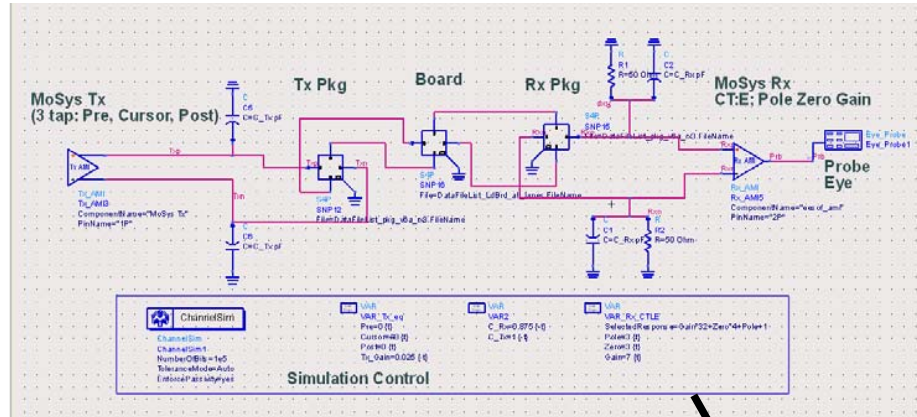
For this analysis, the nominal PZG was 3,3,7. The maximum range for these variables are 4,8, and 16, respectively. Here the Pole, Zero and Gain are varied by -1 for each term, and the sensitivity observed. Clearly the Zero has the maximum sensitivity. Knowing the relative impact, one can focus your efforts on the main variables first.

Figure 30   Paretto showing sensitivity (%) of RX Pole, Zero, and Gain parameters.
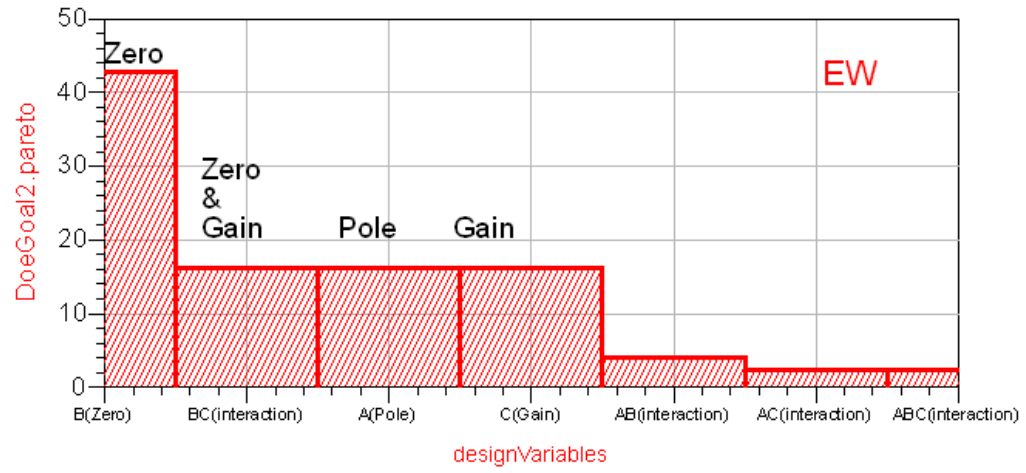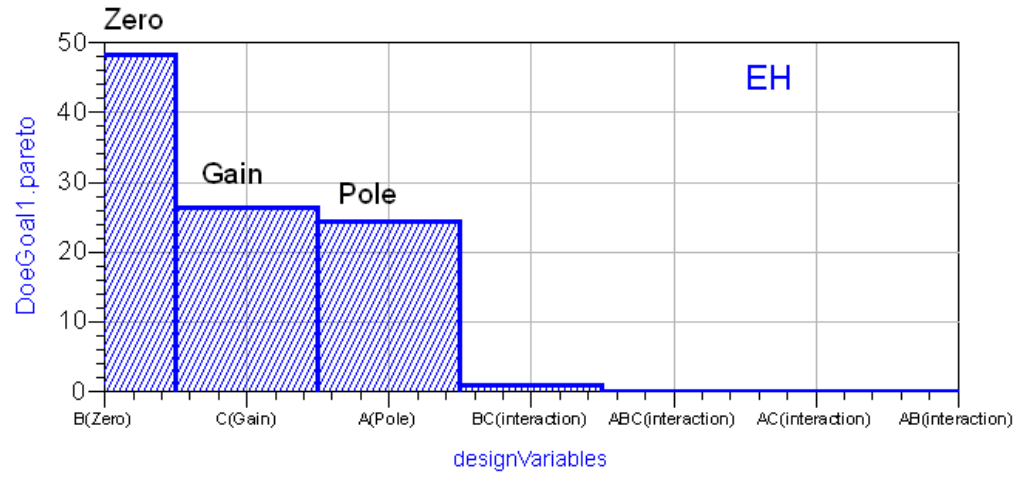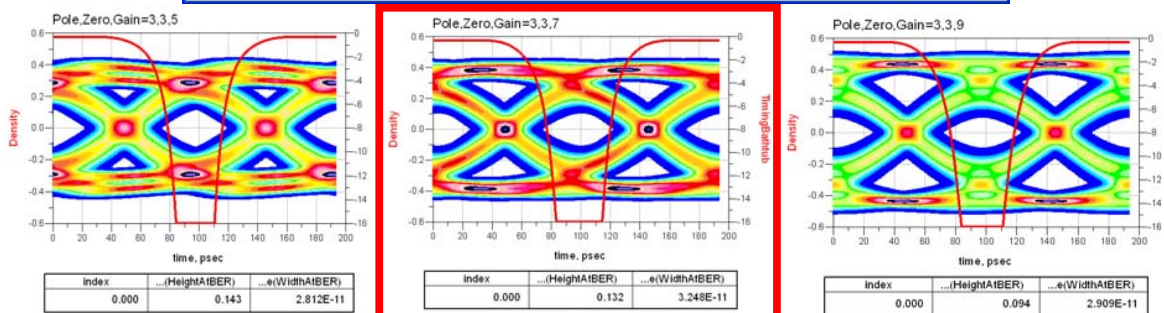
Interactive Tuning

Figure 31 Interactive tuning example. The tuning variables are tuned and the resulting eye is observed interactively, and retuned. Several snapshots of the eye as a function of "Gain" are shown below, with the "Gain" at 7 as the optimum for this simulation.


Batch Simulation

In the batch simulation, all the relevant variable combinations are swept. The result is processed and analyzed after the simulation is completed. An example of such a representation is shown in Figure 32. This shows that a gain of "6" is optimum for eye height, whereas "7" is best for width.

Figure 32 Eye height and width as a function of "Gain" parameter.
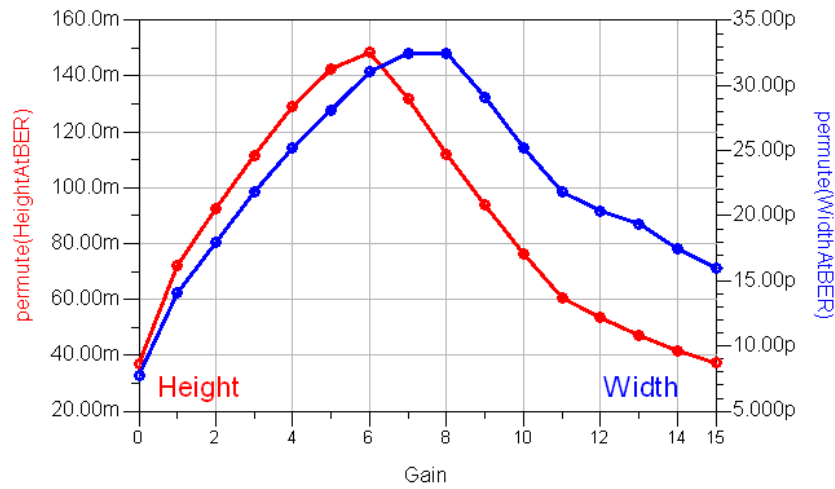
Another representation of the data is a surface or a contour as shown in Figure 33. Here two variables optimization can be conveniently made.

Figure 33 Example of a contour plot showing simultaneous sweeping of "Zero" and "Pole", showing the optimized contour for eye width.
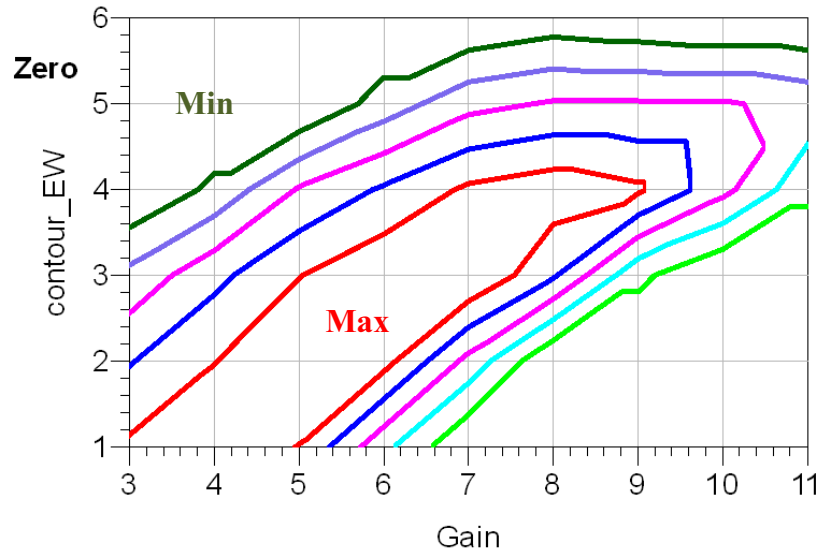

Goal-based Optimization

In this process, first the optimization variables are defined, then the goals are specified. Typically the optimization variables are the equalizer control, swing control, and so forth, whereas the goals can be eye height, eye width, and TX swing (for power).

The analysis may be over a number of conditions, as well as interconnect. An overall optimum can be sought.

Figure 34 Optimization control example

Figure 35 Example of a goal-based, multi-variable optimization.
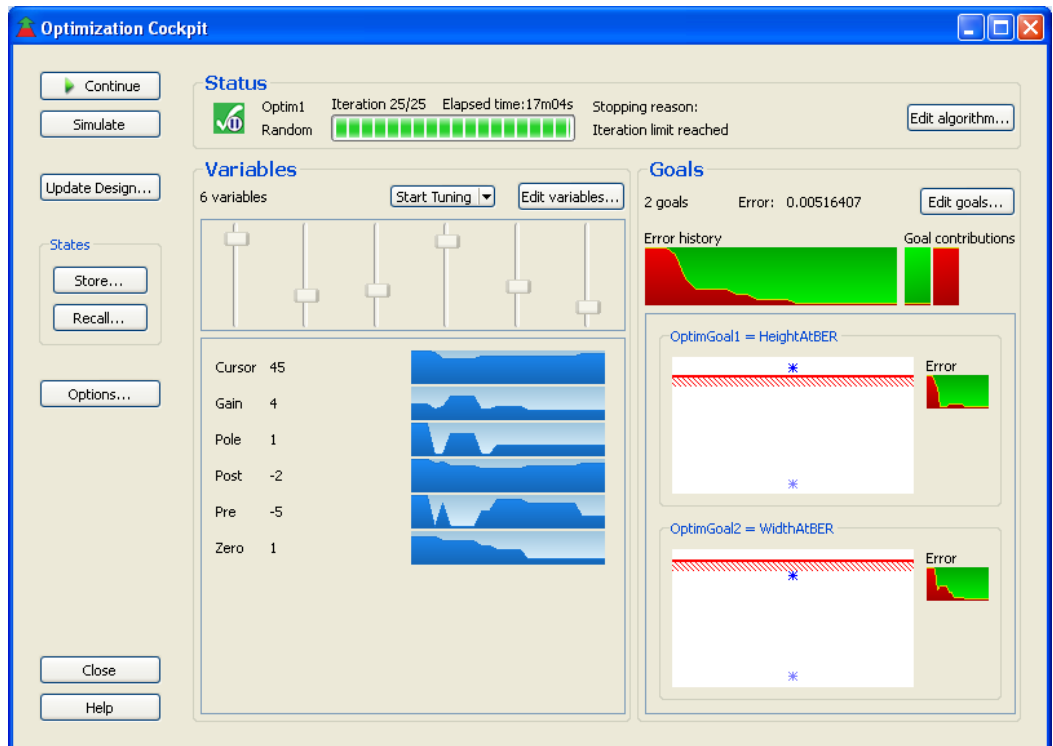
Version History

Date	Version	Changes
July 2011	0.1	Initial release.
Jan 2013	0.2	Update tables 6 and 7

1/21/13

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