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Peraso Quazar QPR (Quad Partition Rate) and Blazar (Bandwidth Engine) Serial High-Speed Memory ICs Product Brief

SERIAL ACCELERATOR ENGINE IC INTRODUCTION

Peraso is the leader in high speed serial memory. The Quazar & Blazar family of high access rate, high capacity serial memory ICs solve critical memory access bottlenecks in data processing and compute applications. Designers often need to extend their onchip SRAM and use these devices for any FPGA/ASIC designs that require external memory support from 50Gbs to over 400Gbs per device.

Two Device Families:

- **Quazar (QPR: Quad Partition Rate)** – fast SRAM functionality, ideal for QDR replacement
- **Blazar (BE: Bandwidth Engine)**: same as Quazar but adds Burst for high-speed Reads & Writes, and on-chip ALU for Read-Modify-Write (RMW) functionality

KEY FEATURES

- High Bandwidth (Up to 400Gbs)
- Up to 6B transacations/second single device
- High access rate SRAM memory (2.7ns tRC)
- 576Mb/1.1Gb capacity single package (8x QDR)
- Highly efficient command and data protocol (optimized for memory transactions)
- Serial interface (10-25Gbps SerDes)
- 4 -16 SerDes lanes to FPGA (vs. 100's of GPIOs)
- Internal RMW Macro functions for statistics, metering, filtering, atomics operations
- Interoperable with Achronix, Intel, Xilinx FPGAs
- Memory controller provided

PRODUCT OPTIONS:

Quazar (QPR) - Serial Memory IC: (QDR SRAM Replacement):

- Serial memory with high access Read/Write commands
- Benefits: High Bandwidth / fewer pins, removes memory access bottlenecks, 3-6B transactions per second, high performance, small package size
- Applications: Fast Buffers (Video, Oversubscription…), Table Lookup (Security, Queue, Search)

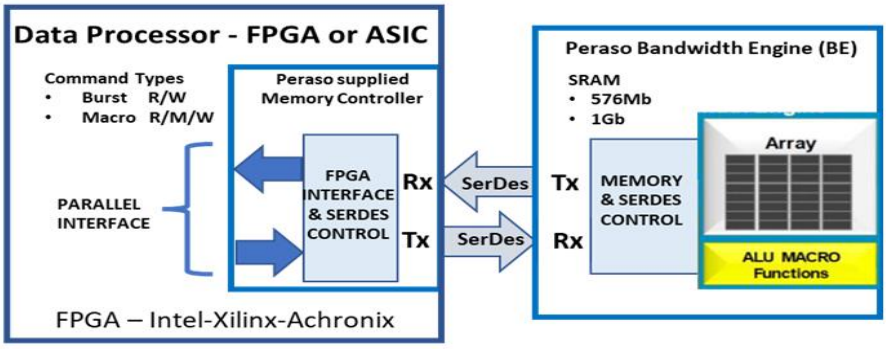
Blazar (BE) Accelerator Engine IC: (Intelligent Memory) – Same as Quazar but adds on-chip functions:

- Supports Burst accesses of 2 to 8 words
- Adds ALU for RMW commands
- Benefits: 4-8x reduction in RMW transactions, lower complexity for host Integrated statistics, metering
- Applications: Statistics, Security (Packet, data, state), Metering (Dual Leaky bucket)

BENEFITS: SERIAL vs PARALLEL MEMORY

- Leverages FPGA SerDes
- Dramatically saves GPIOs
- Board Space Savings
- Superior Signal Integrity
- Part Placement Flexibility
- Lower Power
- Saves Design Time

Blazar/Quazar Accelerators



Peraso SRAM Memory Capacity

- QPR4/BE2 576Mb
- QPR8/BE3 1.1Gb

FPGA Devices

- Achronix
- Intel
- Xilinx

ASIC Devices

- With Serdes Interface

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BLAZAR & QUAZAR PRODUCT OPTIONS

In-Memory	Part Number	Description	Package	Interface					Memory		Access Rate		In-Memory Functions	
			Pkg Size	Lanes	Rate per Lane Gb/s				BW MAX.	tRC	Size	Billion Transactions per second	R/W	BURST for Data Movement	RMW / ALU for Compute and Decision
			mm	Tx/Rx	10.3	12.5	15.6	25	Gb	ns	Gb				
QPR4	MSQ220	QPR4 (Quad Partition Rate) 0.5 Gb	FCBGA 19X19	16	✓	✓			320	3.2	0.5	2.5	✓		
QPR8	MSQ230	QPR8 (Quad Partition Rate) 1Gb	FCBGA 27X27	16			✓	✓	640	2.7	1	5	✓		
BURST	MSR622	Bandwidth Engine 2 Burst Serial 0.5Gb High Access Memory	FCBGA 19x19	16	✓	✓			320	3.2	0.5	3.3	✓	✓	
BURST	MSR630	Bandwidth Engine 3 Burst Serial 1Gb High Access Memory	FCBGA 27x27	16		✓	✓	✓	640	2.7	1	6.5	✓	✓	
RMW	MSR820	Bandwidth Engine 2 RMW Serial 0.5Gb High Access Memory with ALU for RMW functions	FCBGA 19x19	16	✓	✓			320	3.2	0.5	3.3	✓	✓	✓
RMW	MSR830	Bandwidth Engine 3 RMW Serial 1Gb High Access Memory with ALU for RMW functions	FCBGA 27x27	16		✓	✓	✓	640	2.7	1	6.5	✓	✓	✓
RTL	RTL-AE	RTL Memory Controller for Bandwidth Engine and Programmable Hyper Speed Engine. Manages memory and the serial interface signals. Presents a QDR like parallel RTL interface to the user.	FPGA RTL Code		✓	✓	✓	✓			576Mb & 1Gb	6.5	✓	✓	✓

BW MAX. = Aggregate of all SerDes laneS at the highest serial interface speed

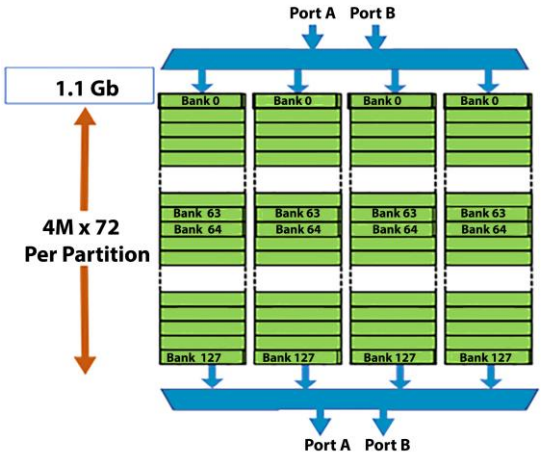
EVALUATION BOARDS & REFERENCE OPTIONS

DUAL PORT CAPABILITY

Two Dual Port Use Cases

*** Access Half the Memory From Each Port**

*** 2 Ports Access the Entire Memory Array**



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