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Peraso Quazar QPR (Quad Partition Rate) and Blazar (Bandwidth Engine) Serial High-Speed Memory ICs Product Brief Peraso Quazar QPR (Quad Partition Rate) and Blazar (Bandwidth Engine) Serial High Speed Memory ICs PB 10.20.22

#### SERIAL ACCELERATOR ENGINE IC INTRODUCTION

Peraso is the leader in high speed serial memory. The Quazar & Blazar family of high access rate, high capacity serial memory ICs solve critical memory access bottlenecks in data processing and compute applications. Designers often need to extend their onchip SRAM and use these devices for any FPGA/ASIC designs that require external memory support from 50Gbs to over 400Gbs per device.

#### **Two Device Families:**

- Quazar (QPR: Quad Partition Rate) fast SRAM functionality, ideal for QDR replacement
- Blazar (BE: Bandwidth Engine): same as Quazar ٠ but adds Burst for high-speed Reads & Writes, and on-chip ALU for Read-Modify-Write (RMW) functionality

#### **KEY FEATURES**

- High Bandwidth (Up to 400Gbs)
- Up to 6B transacations/second single device •
- High access rate SRAM memory (2.7ns tRC)
- 576Mb/1.1Gb capacity single package (8x QDR)
- Highly efficient command and data protocol (optimized for memory transactions)
- Serial interface (10-25Gbps SerDes) •
- 4 -16 SerDes lanes to FPGA (vs. 100's of GPIOs) ٠
- Internal RMW Macro functions for statistics, metering, filtering, atomics operations
- Interoperable with Achronix, Intel, Xilinx FPGAs

**Blazar/Quazar Accelerators** 

Memory controller provided

#### Data Processor - FPGA or ASIC Peraso Bandwidth Engine (BE) Peraso supplied **Command Types** SRAM Memory Controller Burst R/W 576Mb Macro R/M/W 1Gh Array FPGA MEMORY Rx SerDes Tx NTERFACE & SERDES PARALLEL & SERDES CONTROL INTERFACE CONTROL Tx SerDes Rx ALU MACRO Functions FPGA - Intel-Xilinx-Achronix

#### PRODUCT OPTIONS:

Quazar (QPR) - Serial Memory IC: (QDR SRAM **Replacement**):

- Serial memory with high access Read/Write commands
- Benefits: High Bandwidth / fewer pins, removes memory access bottlenecks. 3-6B transactions per second, high performance, small package size
- Applications: Fast Buffers (Video, Oversubscription...), Table Lookup (Security, Queue, Search)

#### **Blazar (BE) Accelerator Engine IC:** (Intelligent Memory) - Same as Quazar but adds on-chip functions:

- Supports Burst accesses of 2 to 8 words
- Adds ALU for RMW commands
- Benefits: 4-8x reduction in RMW transactions, lower complexity for host Integrated statistics, metering
- Applications: Statistics, Security (Packet, data, state), Metering (Dual Leaky bucket)

#### **BENEFITS: SERIAL vs PARALLEL MEMORY**

- Leverages FPGA SerDes
- Dramatically saves GPIOs
- **Board Space Savings** ٠
- Superior Signal Integrity
- Part Placement Flexibility
- Lower Power
- Saves Design Time

#### Peraso SRAM Memory Capacity

- QPR4/BE2 576Mb
- QPR8/BE3 1.1Gb

#### **FPGA Devices**

- Achronix
- Intel
- Xilinx

#### ASIC Devices

With Serdes Interface

## PERASO

In-Memory	Part Num ber	Description	Package	ge Interface Memor							mory	Access Rate		In-Memory Functions	
			Pkg Size	Lanes	anes Rate per Lane Gb/s				BW Max.	BW WAX. tRC Size		Billion		RM BURST for	RMW / ALU for
			mm	Tx/Rx	10.3	12.5	15.6	25	Gb	ns	Gb	Transactions R/W persecond	Data Movement	Compute and Decision	
QPR4	M SQ220	QPR4 (Quad Partition Rate) 0.5 Gb	FCBGA 19X19	16	1	1			320	3.2	0.5	2.5	1		
QPR8	M SQ230	QPR8 (Quad Partition Rate) 1Gb	FCBGA 27X27	16			1	*	640	2.7	1	5	1		
RMW BURST	M SR622	Bandwidth Engine 2 Burst Serial 0.5Gb High Access Memory	FCBGA 19x19	16	1	1			320	3.2	0.5	3.3	1	~	
	M SR630	Bandwidth Engine 3 Burst Serial 1Gb High Access Memory	FCBGA 27x27	16		1	1	1	640	2.7	1	6.5	1	1	
	M SR820	Bandwidth Engine 2 RMW Serial 0.5Gb High Access Memory with ALU for RMW functions	FCBGA 19x19	16	1	1			320	3.2	0.5	3.3	1	1	~
	M SR830	Bandwidth Engine 3 RMW Serial 1Gb High Access Memory with ALU for RMW functions	FCBGA 27x27	16		1	1	~	640	2.7	1	6.5	1	1	~
RTL		RTL Memory Controller for Bandwidth Engine and Programmable Hyper Speed Engine. Manages memory and the serial interface signals. Presents a QDR like parallel RTL interface to the user.	FPGA RTL Code		~	~	~	*			576Mb & 1Gb	6.5	1	~	~
		E	W MAX. = A	ggregate	of all Se	rDes la	ineS at	thehi	ghest ser	rial in	terface sp	peed			

### **BLAZAR & QUAZAR PRODUCT OPTIONS**

## EVALUATION BOARDS & REFERENCE OPTIONS

### **DUAL PORT CAPABILITY**

Two Dual Port Use Cases \* Access Half the Memory From Each Port \* 2 Ports Access the Entire Memory Array



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