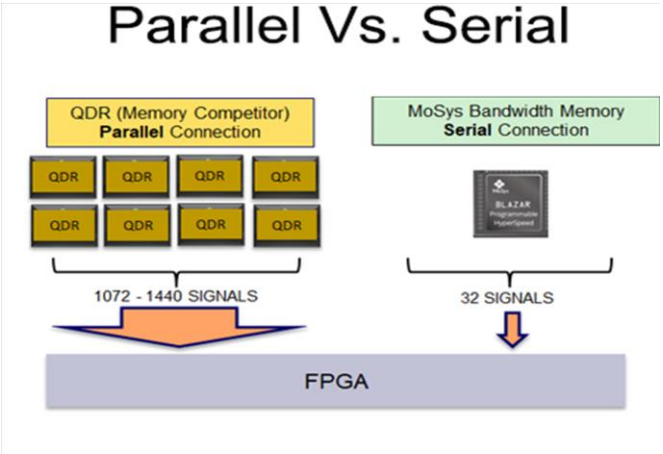
Top Ten Ways to Extend Your Design:
MoSys QPR High Speed SRAM Solutions

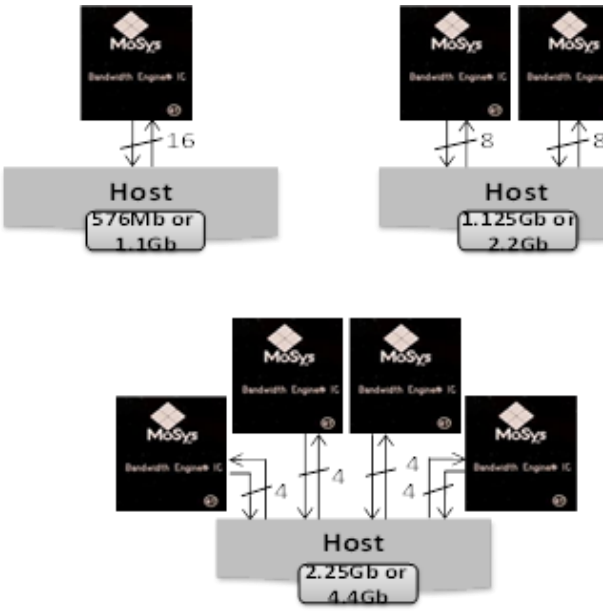
Design Guide

With chip shortages growing daily, more and more customers are looking for ways to extend the life of their designs in ways that save money, improve performance, and reduce design time. MoSys has a number of ways to help customers extend their designs including:

1. MoSys QPR devices can easily replace QDR devices with a density of up to 4x to 8x of a QDR. Instead of buying more memory, the MoSys solution can extend the memory and functionality of a current design. As an example, using MoSys QPR enables 4-8x the number of counters than is normally offered in the system.
2. MoSys QPR devices utilize the ubiquitous SerDes lanes available on today's FPGAs. New ASICs and FPGAs continue to add more and more SerDes lanes available. They are compact, high speed and allow the design to leverage an underutilized resource.
3. The MoSys QPR provides 576Mb or 1.1Gb of high-speed random-access memory in one monolithic package. To achieve this kind of density in a design, it would require 4 to 8 QDR devices and take up much more board space and power.



4. The SerDes I/O allows for flexibility of the MoSys part placement on a PCB, which can be up to 10 inches away from the host device. This helps with PCB layout and power density concerns. All these high-power devices on a card including the FPGA can force a designer to group high-power devices together close to the FPGA. This means 100s of watts of power dissipated in a tight space which needs to be cooled. Utilizing SerDes on the memory devices allows greater placement options on the board to distribute power dissipation more efficiently.
5. Using SerDes lanes makes it possible to tune the access bandwidth of the QPR by utilizing as few as 4 and as many as 16 lanes per device. This allows the designer to tweak the design, choosing the number of lanes needed to achieve the desired bandwidth.



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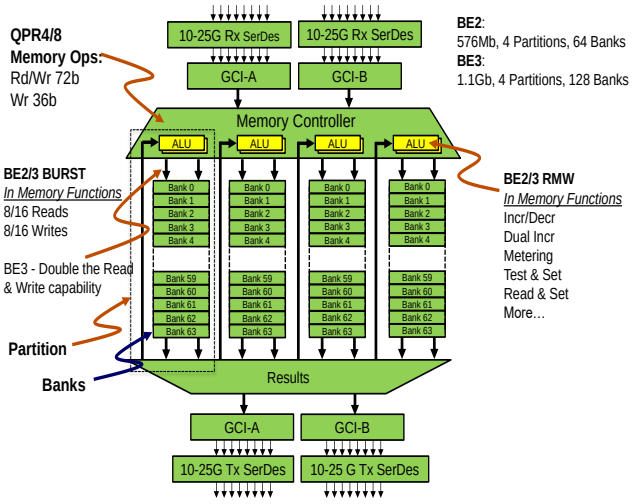
6. MoSys provides (free of charge) a sample FPGA controller (RTL code) which saves costly and valuable development time.
7. Interface speeds of 10Gbps SerDes up to 25Gbps SerDes are available to support data throughput rates of up to 400Gbps (in a single device). This means whatever SerDes are available, the MoSys QPR can cleanly interface to them.



8. Each QPR device has two interface ports (serial GigaChip Interface) allowing for a Dual Ported Functionality. The design can have two different hosts (eg; 2 FPGAs) that talk to one memory.
9. MoSys is available to support both schematic and layout reviews of MoSys devices in a design. Utilizing MoSys's team of experts enables designers to shorten time to market and cut design cycle time.
10. MoSys QPR devices are pin and power rail compatible with MoSys Bandwidth Engine (BE) devices which have greater functionality. So, architects have an upgrade path for higher functionality without having to change their PCB design.

Need more resources or information? Check out:

How Board Design Can Expedite Your Next Design Project Part 1
How Board Design Can Expedite Your Next Design Project Part 2
Why Use SerDes to Talk to Memories? – Part 1 of 2
Why Use SerDes to Talk to Memories? – Part 2 of 2
Why is QDR is No Longer the Answer
One Device Using 32 I/O Pins that Replaces 4 to 8 QDR Devices
MoSys New Quazar Solutions: 4 to 8 times as Many QDR SRAMs in a Single Package
New Quazar Family of High-Speed SRAMs from Mosys Part 1 of 2
New Quazar Family of High-Speed SRAMs from Mosys Part 2 of 2
Memory Controllers Part 1 of 2
Memory Controllers Part 2 of 2

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