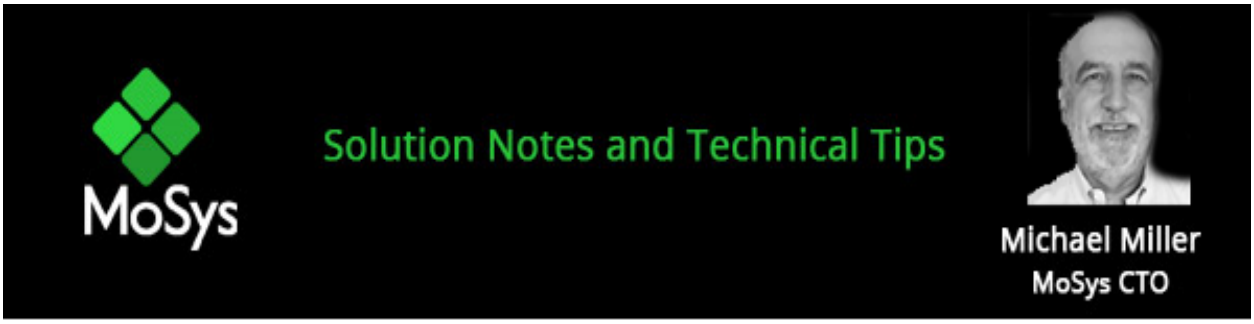


SOLUTION NOTE #1006 Comparison of Bandwidth Engine to Other Memory Solutions
TOPIC SUMMARY:

Overview

Memory Comparison

In this solution note we will compare the most common memories that we see used in high-speed memory applications and then review how the MoSys Bandwidth Engine Family of memories compare. As is apparent to many, there does not seem to any one device that can cleanly handle all application requirements. We will therefore review what have recently been the most common device types used.

DRAM

DRAM is a great general-purpose memory solution that was developed to address large capacity, reasonably low power and low-cost requirements (especially DDRx due to its use in a broad set of applications, from gaming systems to high performance computing). Each of which has differing requirements and therefore the need to use different memories and many times multiple types of memories to address different system requirements. As you can see in the comparison chart of key attributes below, if the application can tolerate tRC in the range of 40ns and there is no need for an access pattern that requires quick and random access, then a DRAM option is a very viable alternative to other memories. This can rightfully lead to a conclusion that if the application performance can be met with low-cost DRAM without going through significant pain, it is most likely a benefit to use it.

However, there are also a significant set of applications that are concerned with faster access speeds, random access rates and limited I/O pins and board space, all of which are of additional consideration when attempting to decide on memory choices. To support current and future system performance requirements, other options such as higher access rate memories are needed. So, this is where the MoSys Bandwidth Engine fits. The following is a comparison of the MoSys Bandwidth Engine to DRAM:

Comparison of Bandwidth Engine to DRAM (see table below)

Attribute	Bandwidth Engine BE-2 | BE-3		Hybrid Memory Cube (HMC)	High Bandwidth Memory (JEDEC)	DDR4 (JEDEC)
Physical Interface	Serial CEI Standard		Serial CEI Std	JEDEC HBM IO	JEDEC DDR4 IO
Protocol	GigaChip™ Interface		HMC Consortium	RAS/CAS	
Access	TDM	Scheduler	Sched./Switch	Banked RAM	
tRC (memory bank rate)	3 ns	3 ns	~40 ns	~40 ns	~40 ns
Capacity	576 Mb	1152 Mb	16~32 Gb	32-64 Gb	4-8 Gb
Buffer Bandwidth	400 Gbps	800 Gbps	1280 Gbps	1600 to 2048 Gbps	4.8 Gbps
Random Access Rate	>4.5 Bt/s	>10 Bt/s	2.6~2.9 Bt/s	2.5B to 5Bt/s*	0.2 Bt/s
Special Functions	Int RMW functions	Int RMW Functioins	n/a	n/a	n/a
Signal Pins	66	66	272	~1600	42
Package	BGA 19x19	BGA 27 x27	BGA 31x31	KGSD	BGA 8x12
Power	7-11W	18-24W	~28W	Integrated	0.7W + I/O

- DRAM is much denser – measured in Giga**bytes** vs Giga**bits** nearly an order of magnitude denser
- DDR DRAM much cheaper on a cost per bit and per part basis (DRAM leverages commodity markets, lower cost process, doesn't need extra circuits to increase access speed)
    - HBM –High Bandwidth Memory is much more expensive than DDR4, due to the advanced processing required to manufacturer the die
- Bandwidth Engine provides an order of magnitude better Random-Access Rate performance, because there is no tfaw or RAS/CAS to potentially impact an access
- HBM excels with the highest Buffer Bandwidth (Read/Write sequential access)
- Bandwidth Engines support up to 25Gb/s per pair of differential pins with up to 16 per chip
- Pin Count: Bandwidth Engine serial interfaces reduce pin count substantially, which results in a reduce layout complexity
- DDR is lower in overall power, performance of a BE comes at a price of higher power

Applications where the requirements become more demanding and would include >80Gb/s throughput, out of order buffer requirements, maintaining statistics that involve Read-Modify-Write (RMW), Table look-ups, State monitoring, etc., these represent functions that do not easily lend themselves to utilizing DRAM. Occassionally these things can be worked around with maintaining multiple copies in DRAM or a combination of internal SRAM and external DRAM. However, internal SRAM on an ASIC or FPGA is often limited and maintaining memory coherency can consume significant resources and limit performance. In these cases, augmenting or replacing DRAM with higher access-rate memory may be required and beneficial. Below is a comparison of Bandwidth Engine versus the traditional SRAM and RLDRAM alternatives.

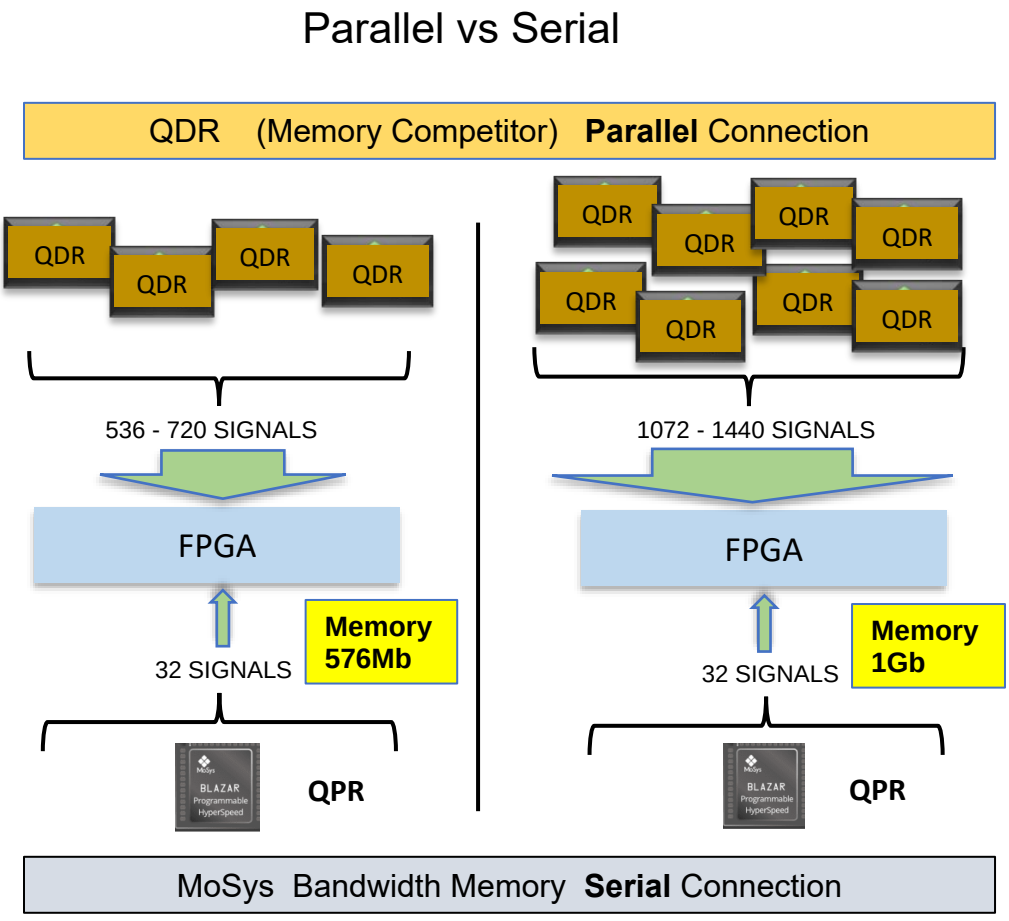
Comparison of Bandwidth Engine to SRAM and RLDRAM (See table below):

Attribute	Bandwidth Engine BE-2 | BE-3		SRAM QDR / Sigma Quad	RLDRAM3
Physical Interface	Serial IEEE / CEI Standard		Parallel	Parallel
Protocol	GigaChip™ Interface		QDR	RLDRAM
Access / Structure	TDM / Partition	Scheduler / Partition	Banked RAM	Banked RAM
Capacity	576 Mb	1152 Mb	72 - 144 Mb	576 - 1125 Mb
tRC (bank access)	3.2 ns	3.2 ns	1.5 -2 ns	7-8 ns
Buffer Bandwidth	400 Gbps	800 Gbps	150 -200 Gbps	86.4 Gbps
Random Access Rate	>4.5 Bt/s	>10 Bt/s	2.0 Bt/s	1.3 Bt/s
Special Functions	Integrated RMW functions	Integrated RMW Functioins	n/a	n/a
Signal Pins	66	66	165	168
Package	BGA 19x19	BGA 27 x27	BGA 13x16	BGA 13.5x13.5
Power	7-11W / IC	18-24 / IC	4.5 – 7W/IC	3.5W / IC

- BE-3 and RLDRAM are the densest, High-Speed devices, SRAM is the smallest
- Cost: RLDRAM is lowest cost per bit, SRAM is the highest cost
- Memory Access Rate: Bandwidth Engine provides 4-8x the access rate of SRAM and RLDRAM
- Raw Bandwidth: Bandwidth Engine gives 4-8x more bandwidth at much lower pin count
- Bandwidth /pin: Bandwidth Engine gives much higher bandwidth per pin with its serial interface
- Pin Count: Bandwidth Engine is much lower and reduces overall pin power
- Power: RLDRAM is lowest power per IC but typically but can end up equal to BE or greater, if multiple devices are needed for performance

Performance

In applications that drive performance, the MoSys Bandwidth Engine gives a 4 to 1 improvement over SRAM for density, or RLDRAM for access rate. SRAM, like a QDR, remains the fastest single access device but is also the lowest density option of the devices we are discussing. It remains a popular option but seems to have reached a terminal point on a product roadmap. At this point, there is no indication that any future devices are being developed. To this end, the MoSys Bandwidth Engine devices offer a great option. The BE-2 device offers the features of higher throughput and 4 times the density of a QDR device. The BE-3 devices offer even greater throughput and 8 times the density of a QDR device. In addition, they offer a presently available option that takes less board space, easier board routing, lower power, and a cost savings, as compared to an equivalent density of QDR devices.



When reviewing the offerings that are currently on the market, we believe that the MoSys family of products offer a superior option and a next generation density and throughput to the following typical application:

1. Fast Buffers: Oversubscription, short term packet storage, video frame buffers, re-order buffers
2. Random Access: Search (LPM, Exact Match…), state tables, flow monitoring
3. Read-Modify-Write: Statistics, counters, metering

If you need to free up resources on your FPGA. or would like more flexibility in your FPGA part selection options, please contact MoSys and we can do a memory architecture design tradeoff review with you. Contact: App Support for a memory architecture discussion! Email us and we will arrange to have one of our technical specialists speak with you. You can also sign up for our Newsletter. Already convinced? You can request a quote from sales. Finally, please follow us on social media so we can keep in touch.