STELLAR Packet Classification Platform IP
Achronix, Intel & Xilinx

PRODUCT BRIEF

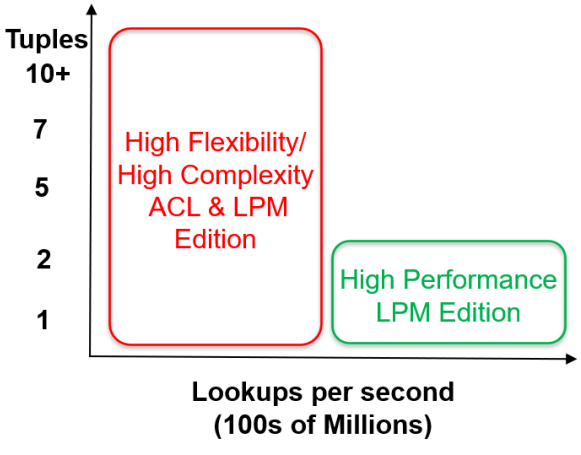
INTRODUCTION

The MoSys STELLAR Packet Classification Platform is provided as IP for a variety of accelerators and supports ultra-high search performance using lookup rules based on highly complex Access Control List (ACL) and Longest Prefix Match (LPM). Stellar supports header lookups at 100s of millions of lookups per second with millions of rules and can easily support networks from 100Gbps to Terabits/s.

Stellar leverages the company's innovative Graph Memory Engine (GME) for performing embedded search and classification of packet headers as an alternative to TCAM functions. The platform includes software that compiles TCAM and search images into graphs for the GME to process.

The Stellar Packet Classification Platform supports multiple different flavors of hardware:

- Optimized RTL IP for FPGA or ASIC
- Software that runs on an x86
- Firmware for the MoSys Programmable HyperSpeed Engine (PHE)



USE CASES & MARKETS

Routing (5G Wireless and Wireline)

- 5G Wireless UPF (User Plane Function) for Edge & Core
- Carrier-Grade NAT
- BNG (Broadband Network Gateway)
- Service Provider / Multi-access Edge
- Cloud / Data Center routing
- Network Classification
- Enterprise Neworking
- Flow Steering, L3 Forwarding & Filtering
- NVFi, vRouter
- Open vSwitch Offload
- Cloud Gateways and more

Security

- Network Next-Gen Firewall (NGFW)
- Access Control Lists (ACLs)
- DDoS prevention
- Allow/Deny Lists
- Network Detection and Response (NDR)
- Anomaly Detection
- Lawful Intercept (LI) and more

Operations

- Application Delivery Controllers (ADC)
- L4 Load balancing
- Network traffic load balancing
- Application and Network Analysis & Telemetry
- Network Traffic Analysis
- Test and Measurement
- Network Packet Brokers (NPB)
- Log File Analysis and more

TWO OPTIMIZED PLATFORMS

MoSys offers two Stellar Packet Classification Platforms that take advantage of MoSys's Graph Memory Engines for FPGA and ASIC that are optimized for very flexible, very complex many tuple lookups using a mix of both ACL & LPM rules or for high performance/high capacity LPM processing.

1) High Flexibility / High Complexity ACL & LPM

- Ultra-High-Speed Search Engine IP
- Ideal for a very wide range of use cases
- Tuned for complex n-tuple lookups using Access Control List (ACL) and Longest Prefix Match (LPM)
- Hundreds of Millions of lookups per second, Millions of Rules
- Optimized for complex 1 - 10+ tuple matches
- Typical key size 40 - 480b keys
- Very fast rule updates - No need to recompile
- On the fly live updates – no need to stop traffic
- Also supports Exact Match

2) High Performance / High Capacity LPM

- Ultra-High-Speed Search Engine IP
- Ideal for very high performance routing
- Tuned for High Performance, High Capacity Routing Lookups using Longest Prefix Match (LPM)
- Hundreds of Millions of lookups per second, Tens of Millions of Rules
- Optimized for 1 or 2 tuple matches
- Typical Key size 40 – 160b, capacities and key sizes beyond normal routing
- Any mix of IPV4 and IPV6 lookups
- Supports virtual routes
- Supports large number of bits for next hop data

COMMON FEATURES

Technology

- Ultra-High-Speed Search Engine IP
- Deep Header Inspection (DHI) solution
- Uses MoSys Graph Memory Engine (GME)
- Common API for software interface – easier to port applications

Performance

- Provides scalable performance
- Low latency solution
- Very efficient memory usage
- Extremely efficient use of logic gates

TCAM Equivalence

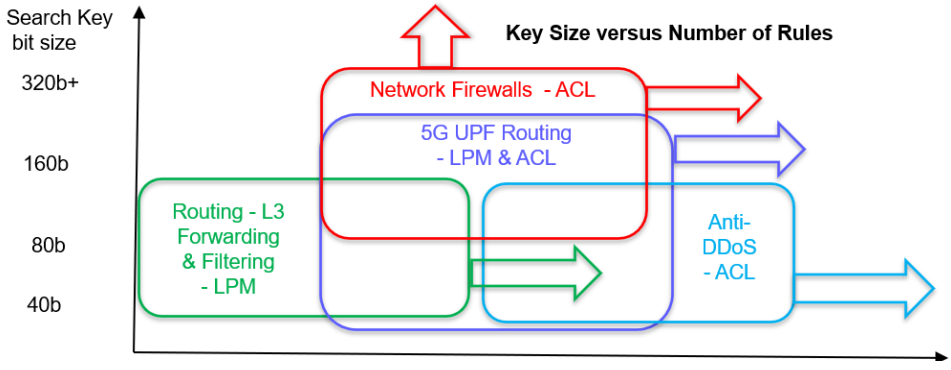
- Replaces multiple expensive and power hungry TCAM chips
- Up to multigigabit TCAM equivalence

Rules

- No need to preconfigure table sizes
- Ability to receive updates from AI/ML logic

Device Support

- Supports Achronix, Intel and Xilinx FPGAs and more
- Can utilize hybrid mix of memories - Internal SRAM and/or external DDR, HBM
- Can also use MoSys memories for even higher performance, but can operate without MoSys silicon
- Available for ASIC, FPGA or software
- Variants use a common API which allows deployment of a wide range of performance points, using the same application code
- Supports ASIC/SoC/DPU/IPU and more
- Applicable to designs based on NIC, SmartNIC, DPU, IPU, Standalone SoC, SmartSwitch and more



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