A Message from MoSys

Welcome to the third edition of the MoSys newsletter. We are excited to bring you a brand-new product line, our new Quazar QPR family of low cost, Quad Partition Rate SRAM Memory ICs.

These new chips are targeted at accelerating Intel and Xilinx FPGA designs at a significant price advantage over traditional QDR SRAMs. *You can replace 4 QDRs for less than $200 in volume quantities!*

Key product features include:
- Less than half the cost of a similar QDR memory configuration
- 4 – 8X QDR Capacity - 567Mb and 1Gb memory options
- Single device replaces multiple QDR parts
- Access to Multiple independent random-access SRAMs on each monolithic device
- tRC of 3.2ns down to 2.7ns
- QDR-like performance and more

So welcome back *to the newsletter where we will continue to keep you up to date on all relevant news.*

Featured Content:

Quazar QPR (Quad Partition Rate) Architecture White Paper
New Quazar Family from Mosys Part 1 of 2
New Quazar Family from Mosys Part 2 of 2
MSQ220 QPR4 Product Brief
MSQ230 QPR8 Product Brief
Quazar Family of QPR Devices

News Alerts!

MoSys Launches New QUAZAR QPR Family of Low Cost, Quad Partition Rate SRAM Memory ICs Targeted for Accelerating INTEL and XILINX FPGA Designs
July 15, 2020

MoSys Announces Availability of its Graph Memory Engine (GME) Accelerator IP Targeting Packet Classification on Intel's Stratix 10 FPGAs
June 8, 2020

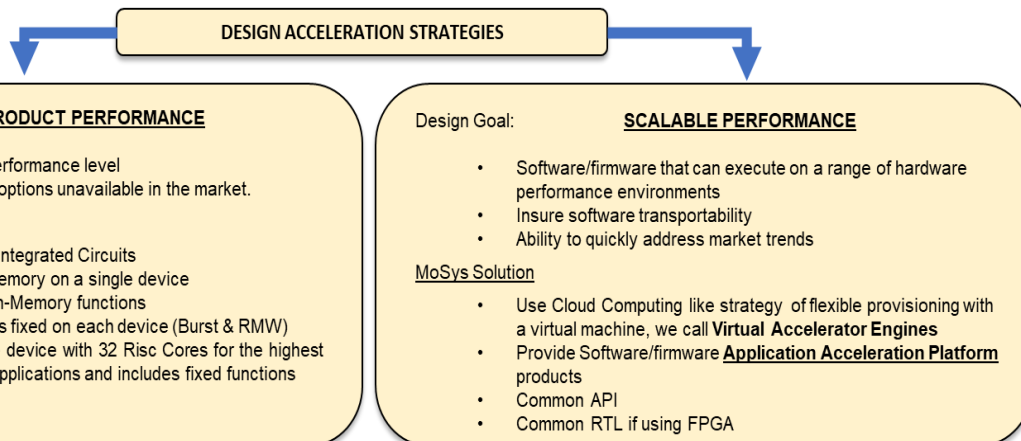MoSys Announces Global Distribution Agreement With Digi-Key Electronics
Mar 3, 2020

MoSys Releases New LineSpeed(TM) 100G PHY Design Support Package
Jan 28, 2020

New Blogs:

- ❖ MoSys Bandwidth Engine vs. QDR
- ❖ An Overview of Graph Memory Engine Technology Part I of 3
- ❖ An Overview of Graph Memory Engine Technology Part 2 of 3
- ❖ An Overview of Graph Memory Engine Technology Part 3 of 3
- ❖ Packet Classification Apps Just Got a Whole Lot Easier to Accelerate and Manage (Again): MoSys New Graph Memory Engine IP Running on Intel's Stratix 10 FPGAs with TDDAM Compiler
- ❖ Do Systems Need SRAMs?
- ❖ Redundant Link Mode with MoSys LineSpeed™ Flex PHY
- ❖ Memory Controllers Part 1 of 2
- ❖ Memory Controllers Part 2 of 2

DESIGN ACCELERATION STRATEGIES

POINT PRODUCT PERFORMANCE

Design Goal:
- System has a target performance level
- Provides Acceleration options unavailable in the market.

MoSys Solution
- **Acceleration Engine** Integrated Circuits
- Largest High-Speed Memory on a single device
- Added intelligence of In-Memory functions
  - Some functions fixed on each device (Burst & RMW)
  - Programmable device with 32 Risc Cores for the highest performance applications and includes fixed functions

SCALABLE PERFORMANCE

Design Goal:
- Software/firmware that can execute on a range of hardware performance environments
- Insure software transportability
- Ability to quickly address market trends

MoSys Solution
- Use Cloud Computing like strategy of flexible provisioning with a virtual machine, we call **Virtual Accelerator Engines**
- Provide Software/firmware **Application Acceleration Platform** products
- Common API
- Common RTL if using FPGA

MoSys Design Support Center

White Paper: Quazar QPR (Quad Partition Rate) Architecture

The Quazar family consists of two parts, QPR4-576Mb and the QPR8-1Gb. These are designed to address the needs for a low-cost next generation of Synchronous SRAM devices on the market. As of the writing of this paper, the device with the largest share of this market is QDR (Quad Data Rate).

The MoSys QPR architecture begins with a focus on solving the issues with the traditional QDR architecture.

- By using the MoSys' 1T memory cell technology, large capacity memories can be created that are able to selectively choose between several modes of operation.

- Using a memory structure built with Partitions and Banks, it allows multiple (4 or 8) independent random-access SRAM memories to exist in one device.

- The flexibility of the architecture allows a single device to achieve a Bandwidth up to 640Gb/s (320 Gb/s full duplex).

- MoSys has architected a device that provides 4 to 8 times the density of a QDR device and achieves this with comparable system latency and 2 to 5 x the system access bandwidth.

- Configurations are a fraction of the cost of a QDR solution.

The QPR design approach that MoSys is presenting is a significant improvement over a standard QDR device.

Link to: [Quazar QPR (Quad Partition Rate) Architecture White Paper](#)
[MSQ220 QPR4 Product Brief](#)
[MSQ230 QPR8 Product Brief](#)

Or, to find out more, Contact: [AppSupport](#)

> **Never miss another newsletter! Sign up for [updates.](#)**

"High-Speed Board Design Guidelines" Up Next: Characteristic Impedance

Many parameters have a strong function of frequency, and it is therefore important to consider frequencies in a wide range vs. only the Nyquist rate (0.5X baud rate).

The common electrical interface spec (CEI Spec, 2014) specifies the insertion and return loss, as a function of the frequency, normalized to the baud rate.

An example of the return loss spec (characteristics impedance match) is shown in Figure 1. For calibration with a single number spec; at the Nyquist frequency of 0.5 the S11 spec from the graph is about -8dB.

Along with the spec, the actual S11 simulation data from two revisions of a PCB board at 28 Gbps (0.5 in the graph corresponds to 14 GHz) is also shown. They both meet the CEI spec. However, the new revision has better impedance matching and will therefore provide more margin to RX, TX or other imperfections in the channel (e.g. vias or connectors).

Link to: ["High Speed Board Design Guidelines"](#)
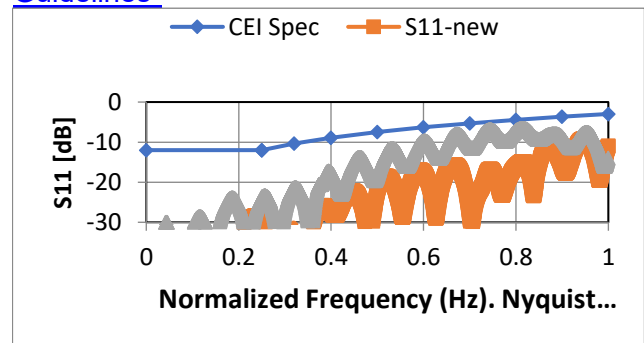
ADDITIONAL RESOURCES
- [Webinar: VAE](#)
- [Solution Note: How Bandwidth Engines (Accelerator Engines) Complement FPGA, BRAM, uRAM](#)
- [White Paper: Chiplet Interconnect – Parallel or Serial?](#)
- [White Paper: Virtualized Acceleration](#)

[Email us](#) and we will arrange to have one of our technical specialists speak with you.. Finally, please follow us on social media so we can keep in touch.